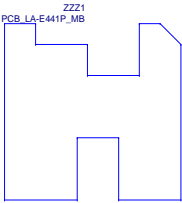


MODEL NAME : ASPEN (CAJ00)
PCB NO : LA-E441P (DAZ1X100100)
BOM P/N :



Dell/Compal Confidential

Schematic Document

ASPEN (Kaby LakeY)

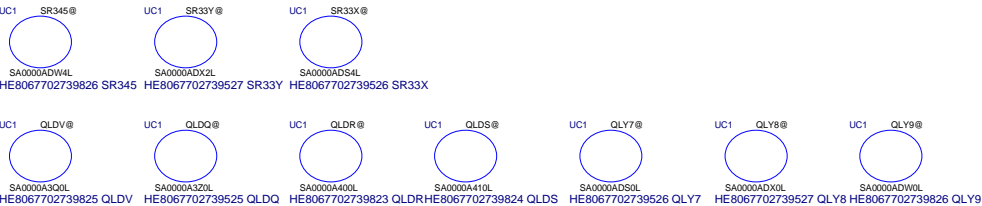
PD Option



AR Option

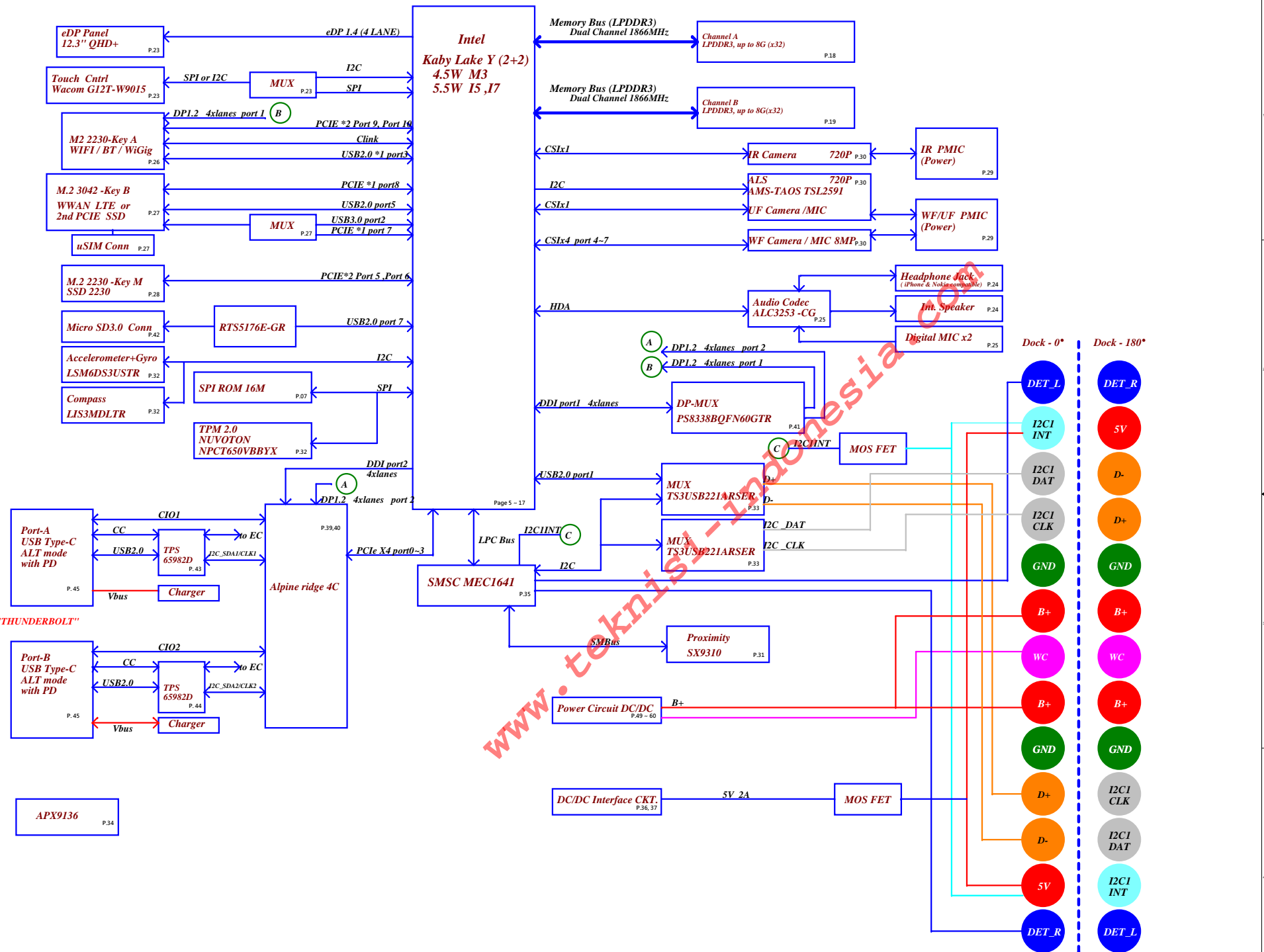


CPU Option

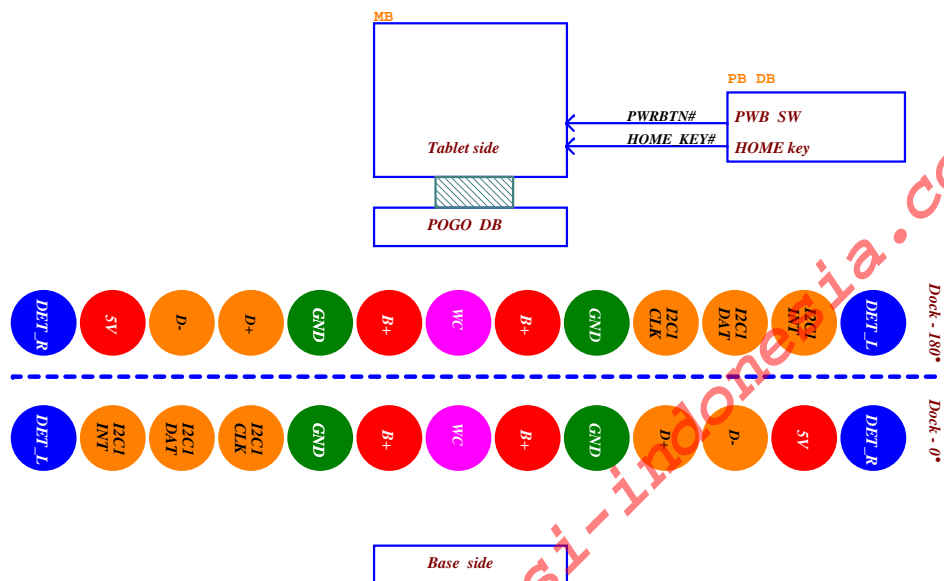


2017-03-23
Rev: 0.6 (A00)

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				LA-E441P	
				Rev 0.10/09	
				Worksheet: March 29, 2017	
				Sheet 1 of 60	



Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	REV	
0	130K +/- 5%	4700p	0.1	EVT1
1	62K +/- 5%	4700p	0.2	EVT1.1
2	33K +/- 5%	4700p	0.3	DVT1
3	8.2K +/- 5%	4700p	0.4	DVT1.1
4	4.3K +/- 5%	4700p	0.5	DVT2
5	2K +/- 5%	4700p		PVT
6	NC			
7				

SMBUS Control Table

	SOURCE	Base	BATT	Charger	TBT	XDP	P-sensor
PCH_SMLCLK PCH_SMLDATA	PCH						
PCH_SML1CLK PCH_SML1DATA	PCH						
MEM_SMBCLK MEM_SMBDATA	PCH					V	
EC_SMB00_CLK EC_SMB00_DAT	MEC1641						
EC_SMB01_CLK EC_SMB01_DAT	MEC1641				V		
EC_SMB03_CLK EC_SMB03_DAT	MEC1641		V				
EC_SMB04_CLK EC_SMB04_DAT	MEC1641			V			
EC_SMB05_CLK EC_SMB05_DAT	MEC1641	V					
EC_SMB07_CLK EC_SMB07_DAT	MEC1641						V

FLEX CLOCKS	DESTINATION
CLKOUT_LPC_0	EC LPC
CLKOUT_LPC_1	BIOS Debug

USB 3.0 PORT#	DESTINATION
1	Debug
2	WWAN

USB 2.0 PORT#	DESTINATION
1	BASE
3	BT
5	WWAN
9	Debug

PCH DDI Port Mapping	DDI PORT#	DESTINATION
	B	DP MUX
	C	TBT
	D	

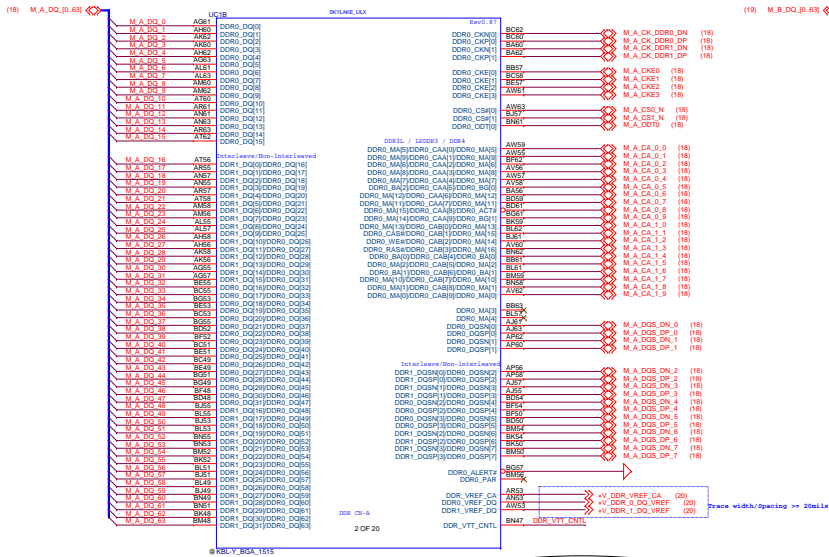
PCI EXPRESS	DESTINATION
Lane 1	TBT (Alpine Ridge, Gen3)
Lane 2	TBT (Alpine Ridge, Gen3)
Lane 3	TBT (Alpine Ridge, Gen3)
Lane 4	TBT (Alpine Ridge, Gen3)
Lane 5	SSD (NGFF, Gen3)
Lane 6	SSD (NGFF, Gen3)
Lane 7	2nd SSD (Gen3)
Lane 8	WWAN (NGFF, Gen3)
Lane 9	WIGIG (NGFF, Gen2)
Lane 10	WLAN (NGFF, Gen2)

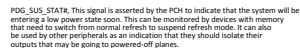
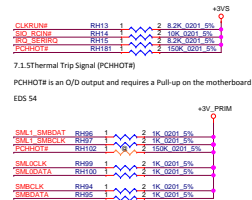
CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE1	TBT
	CLKOUT_PCIE2	WIGIG
	CLKOUT_PCIE3	PCIE SSD
	CLKOUT_PCIE4	NGFF (WLAN)
	CLKOUT_PCIE5	2nd SSD

Symbol Note :

- @ : means de-pop
-  : means Digital Ground
-  : means Analog Ground

Non-interleaved Memory





PDG_SUS_STATE. This signal is asserted by the PCH to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes.

Functional Strap Definitions

GPP_C5 (Internal Pull Down): SML0ALERT#

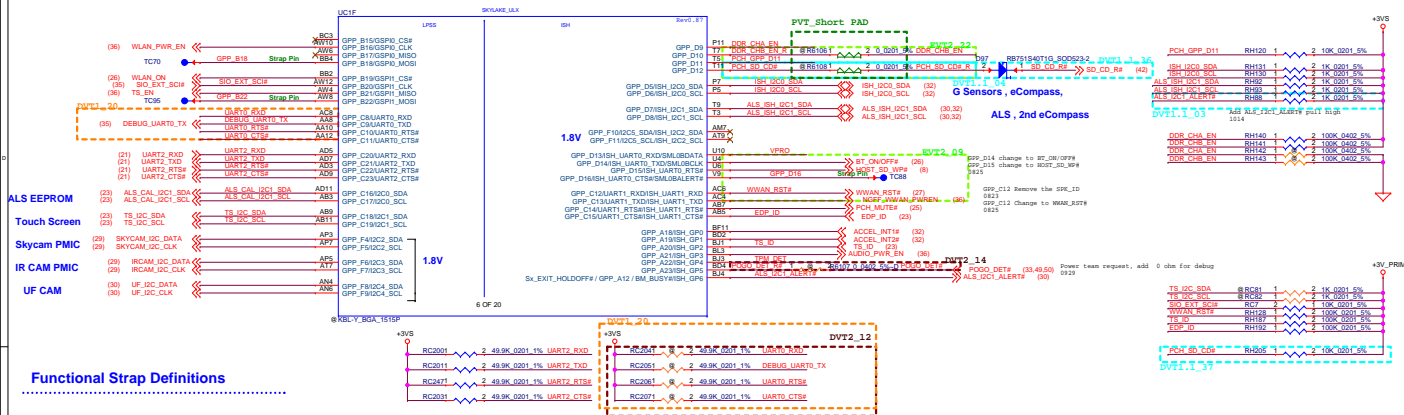
0 = LPC Is selected for EC.

1 = eSPI Is selected for EC.



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Date			Wednesday, 28 Jul 2017	Sheet 7 of 60



Functional Strap Definitions

GPP_B14 (Internal Pull Down): SPKR

TOP Swap Override

0 = Disable TOP Swap mode. -> CAJ00 Use

1 = Enable TOP Swap Mode.

GPP_B18 (Internal Pull Down): GSSPIO_MOSI

No Reboot

0 = Disable No Reboot mode. -> CAJ00 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running TP7XDP.

GPP_B22 (Internal Pull Down): GSSPI0_MOSI

Boot BIOS Strap Bit

0 = SPI Mode -> CAJ00 Use

1 = LPC Mode

GPDP16 (Internal Pull Down):

eSPI or LPC

0 = LPC is selected for EC -> For KB9022/9032 Use

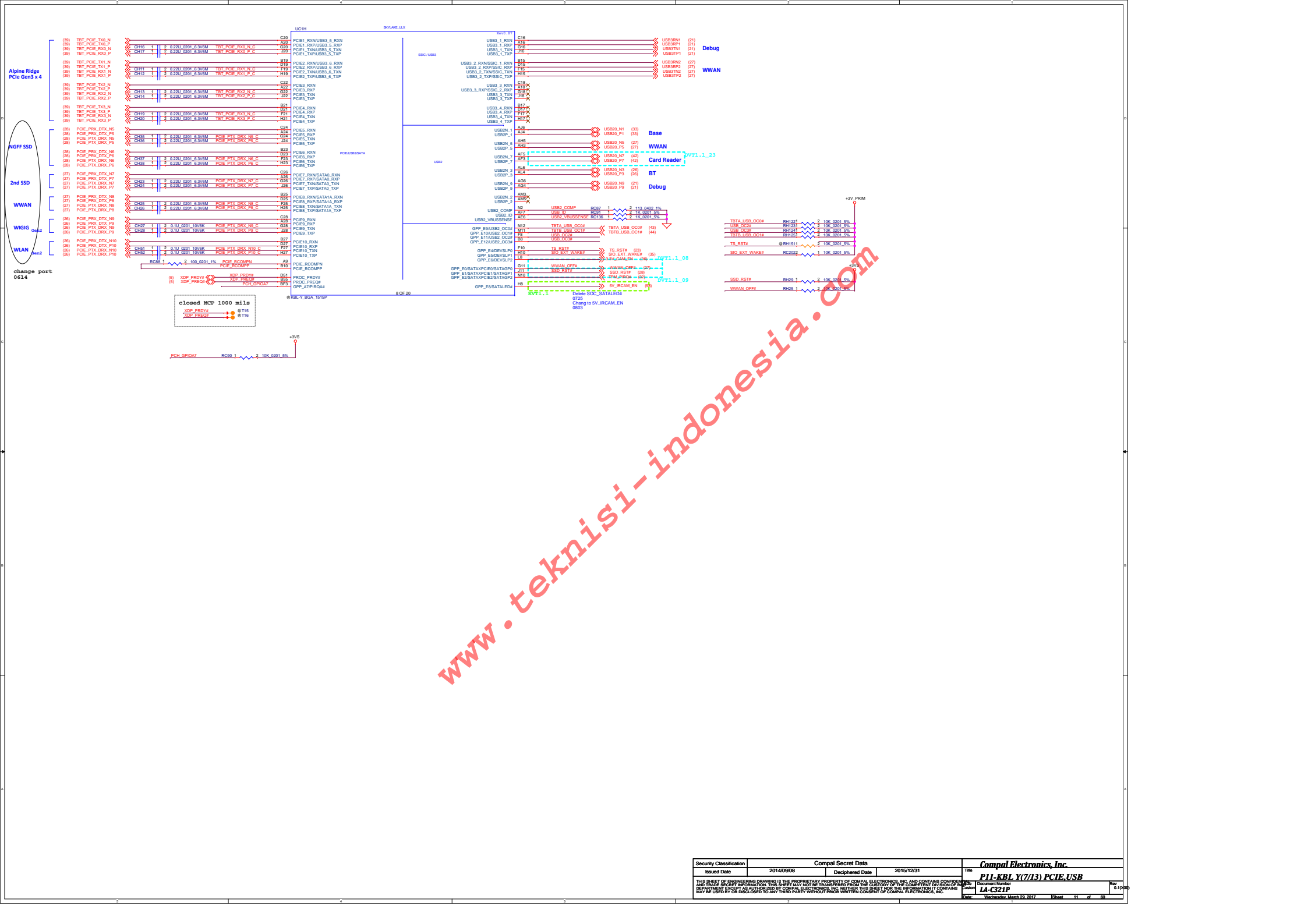
1 = eSPI is selected for EC -> For KB9032 Only.

VPRO BOM Optional

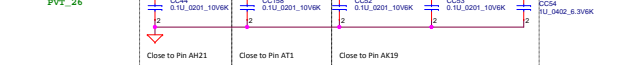
VPRO
1 = W/VPRO
0 = W/O VPRO

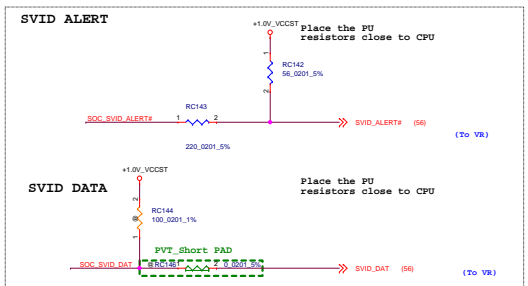
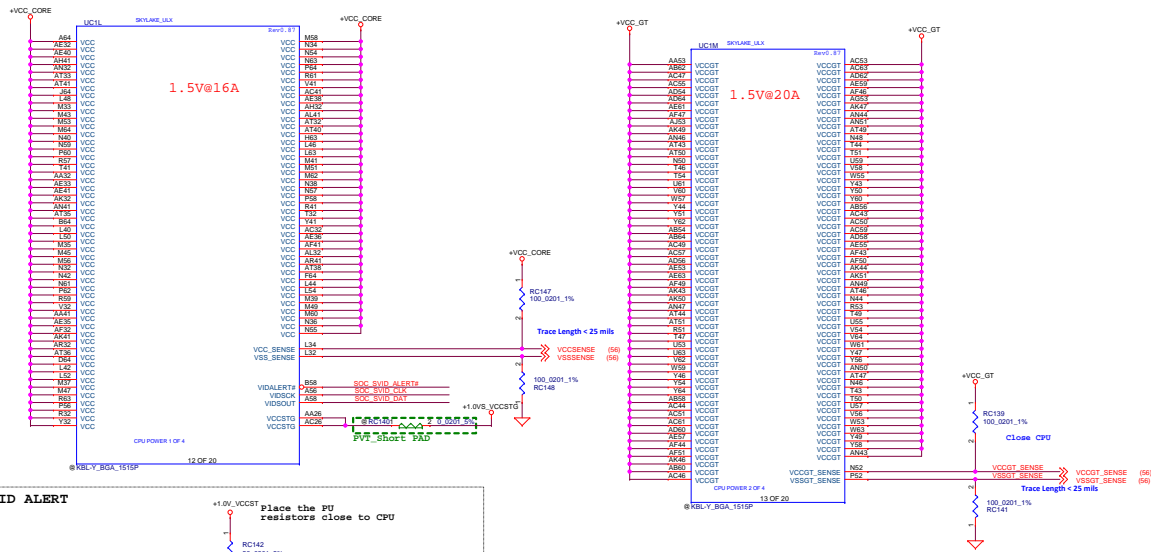
TPM DET BOM Optional

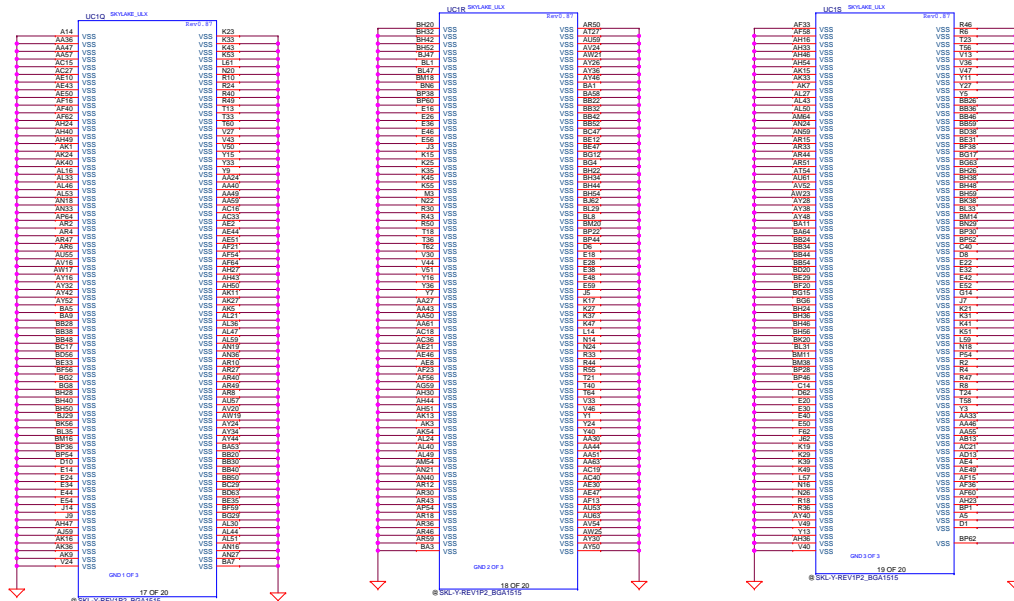
TPM_DET
1 = W/TPM
0 = W/O TPM



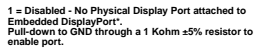
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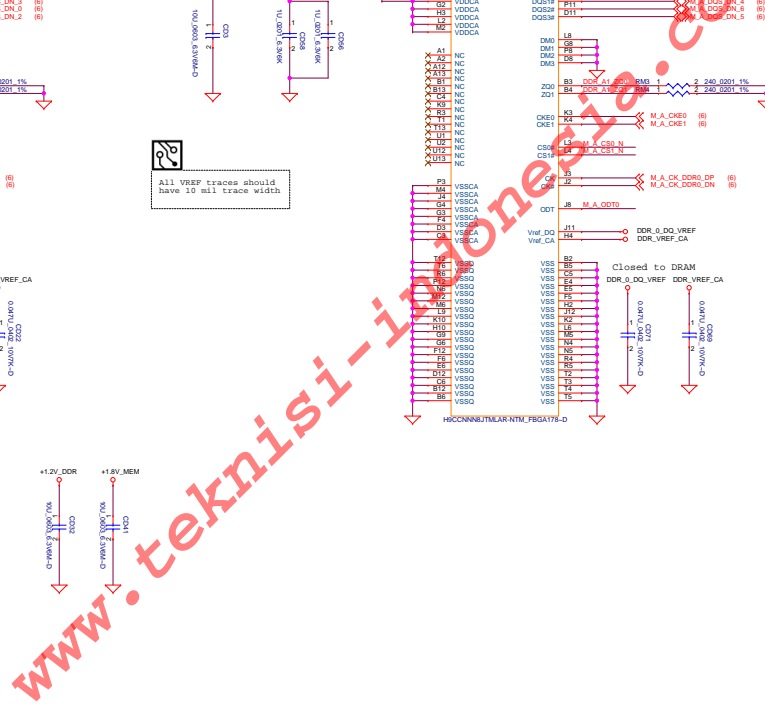


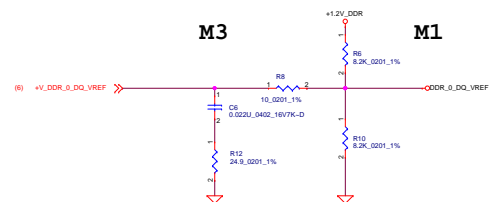




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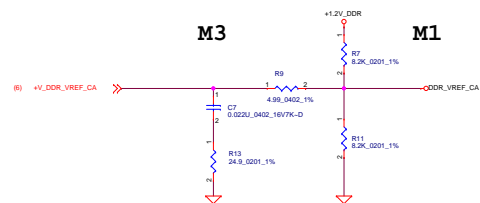
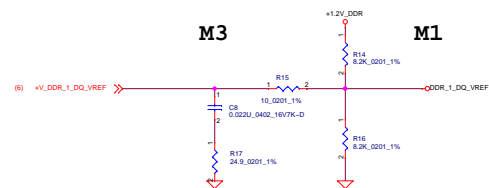






All VREF traces should
have 10 mil trace width

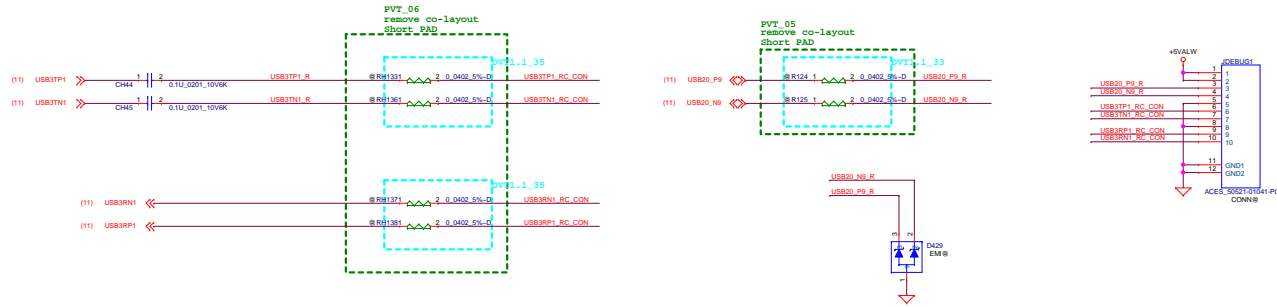
Place the VREF voltage divider as close as possible
to the LPDDR3 x32 memory down DREM devices



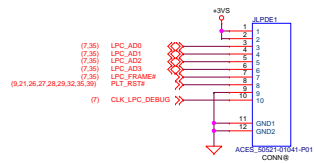
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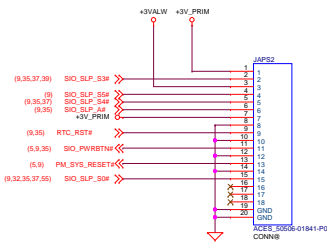
WIN debug



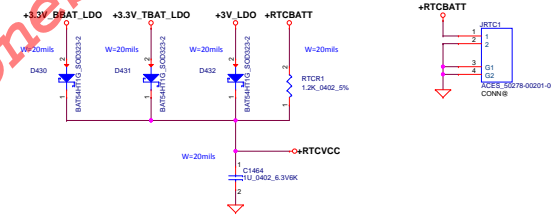
BIOS debug



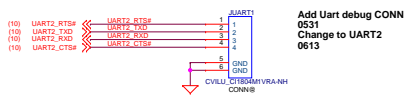
APS



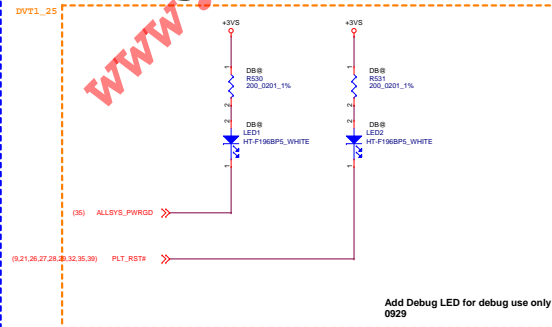
RTC

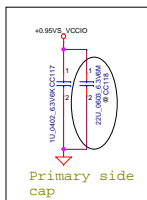
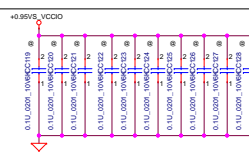
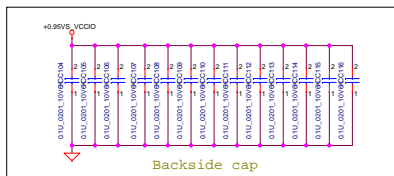
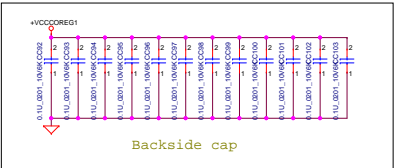
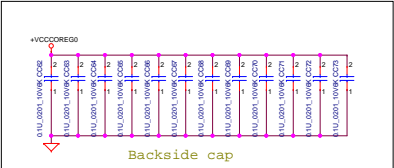


BIOS UART debug

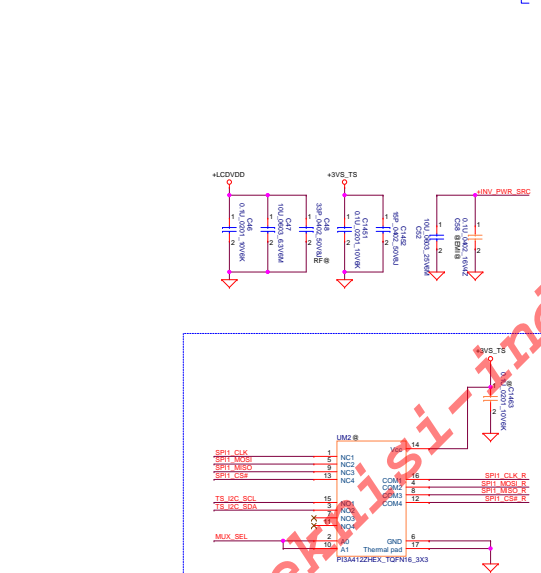
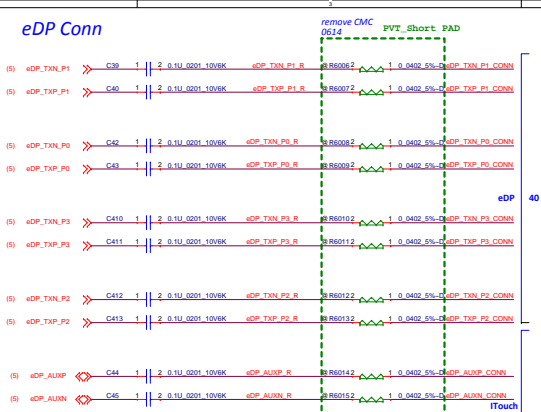
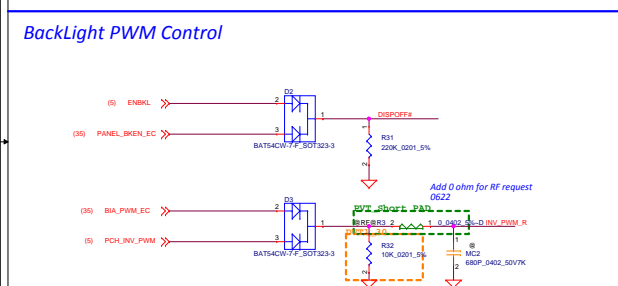
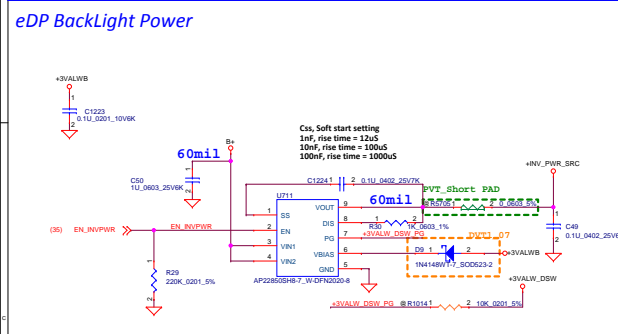
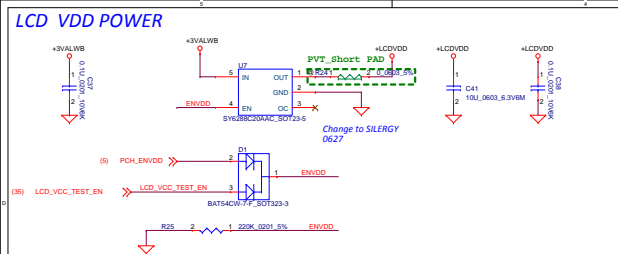


Debug LED





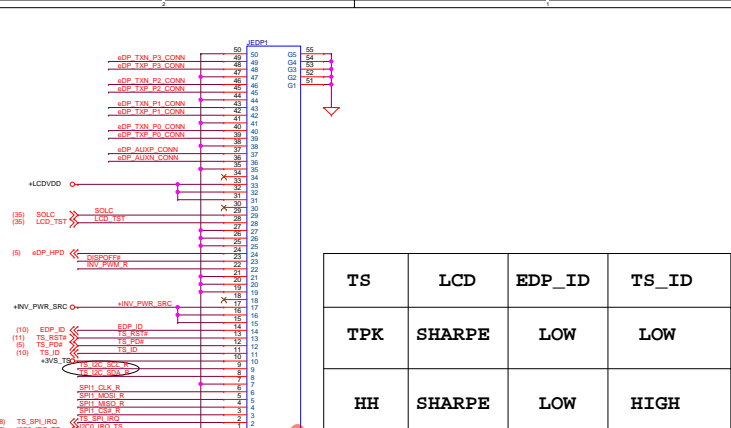
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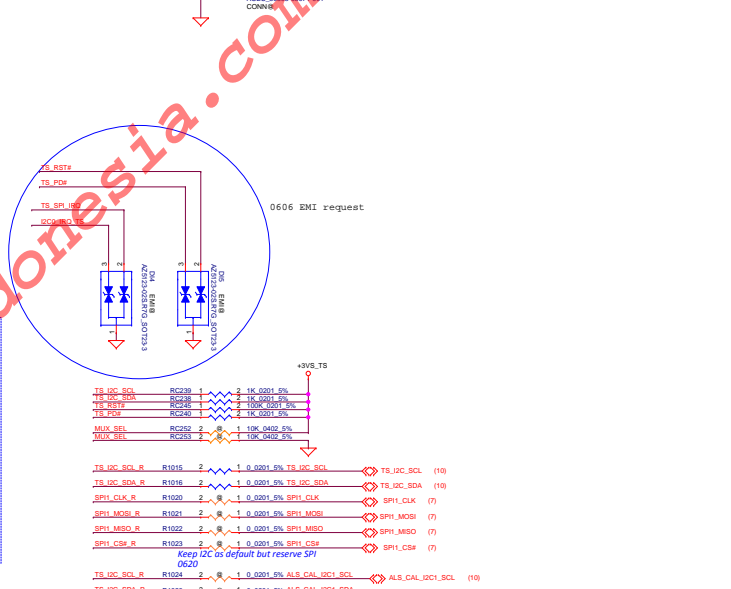
Logic Function Table

Logic Input (IN _x)	Function
0	NC _x Connected to COM _x
1	NO _x Connected to COM _x

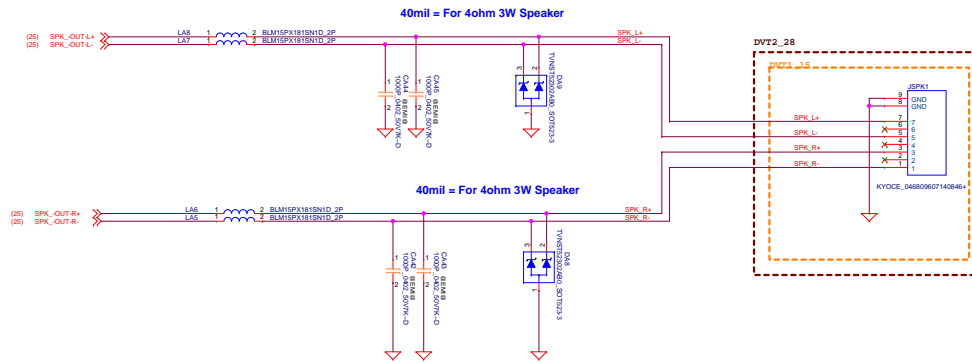
Note: x = 1, 2, 3 or 4



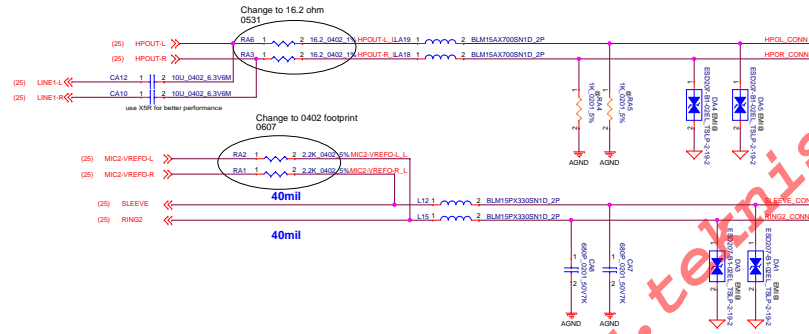
TS	LCD	EDP_ID	TS_ID
TPK	SHARPE	LOW	LOW
HH	SHARPE	LOW	HIGH



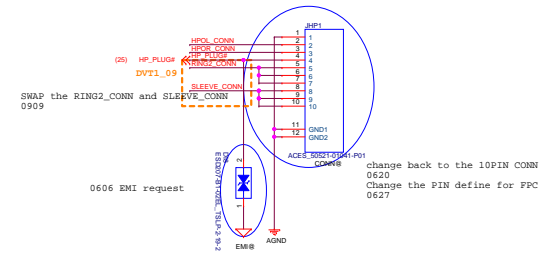
Int. Speaker Conn.



Universal Audio Jack

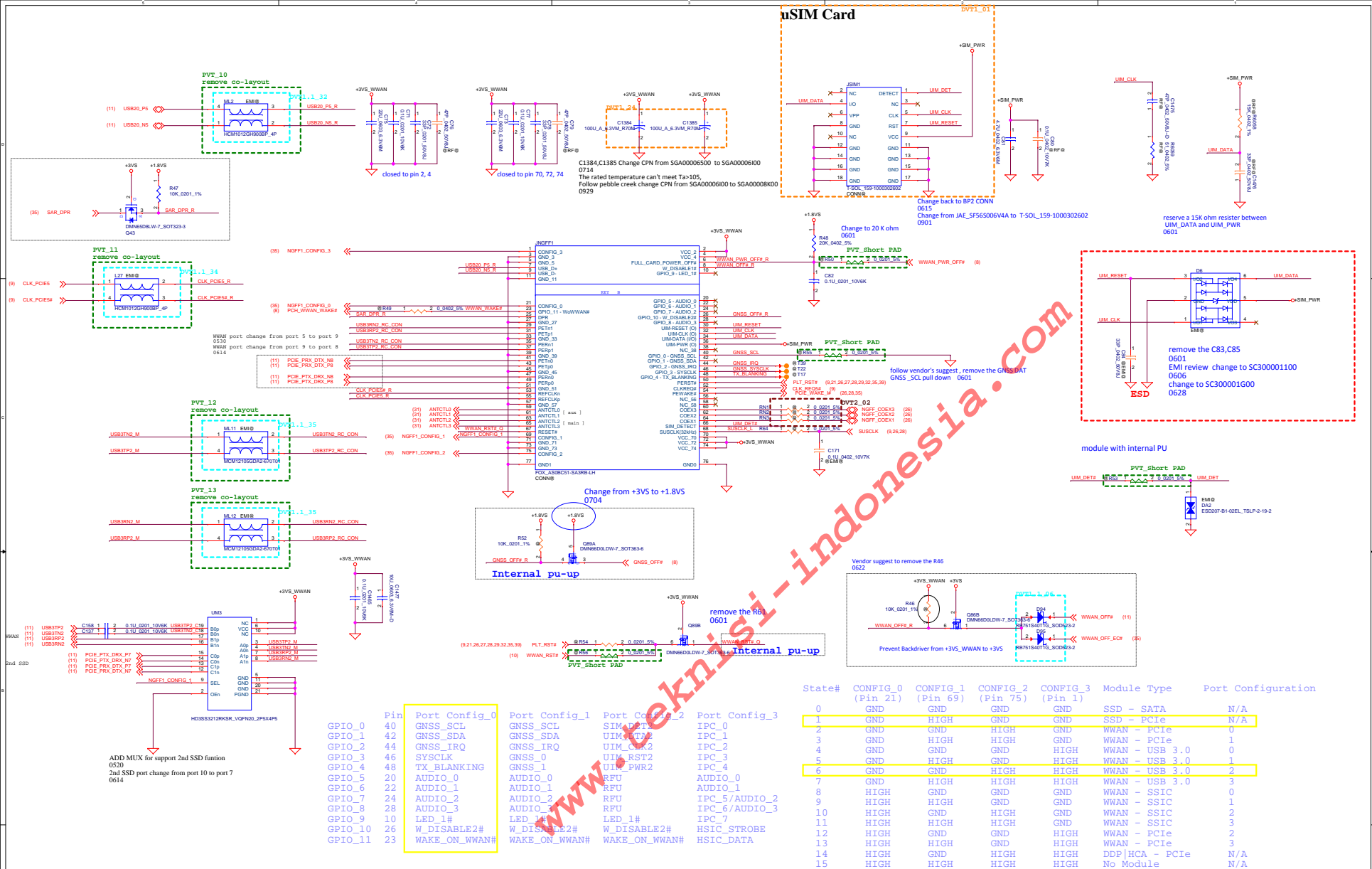


Universal Audio Jack CONN



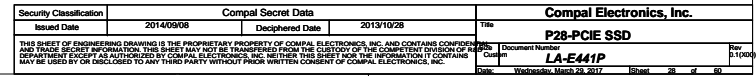
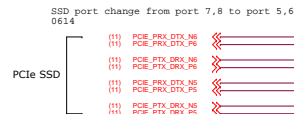
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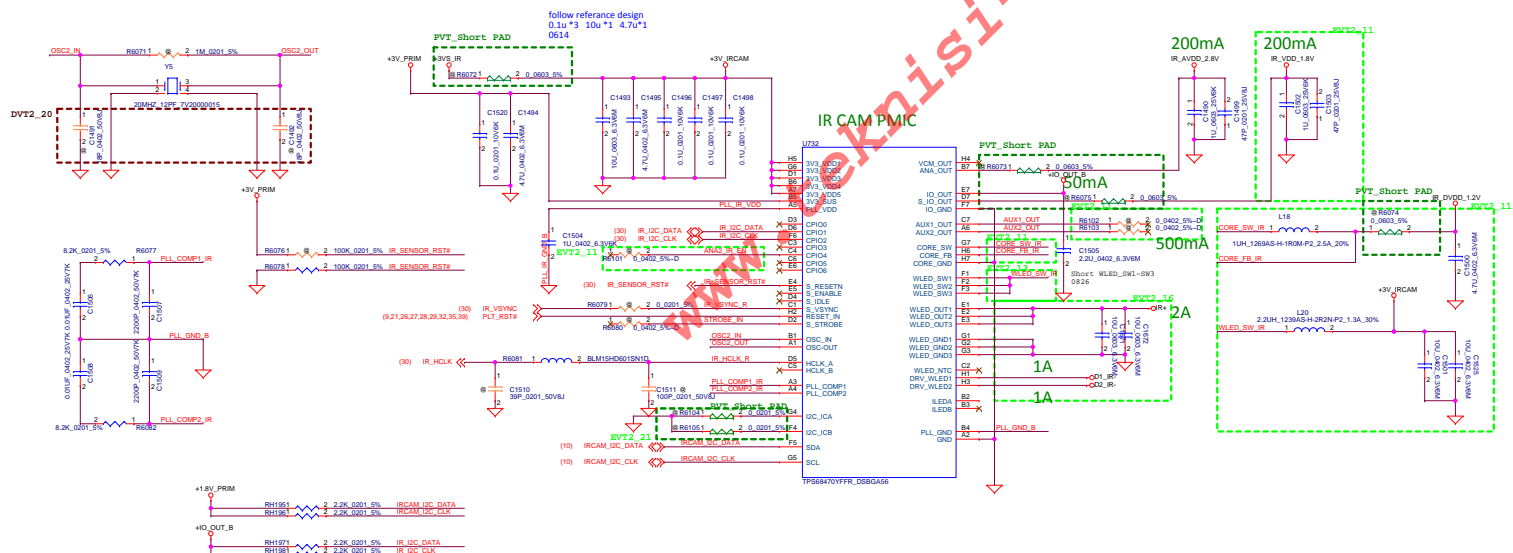
uSIM Card



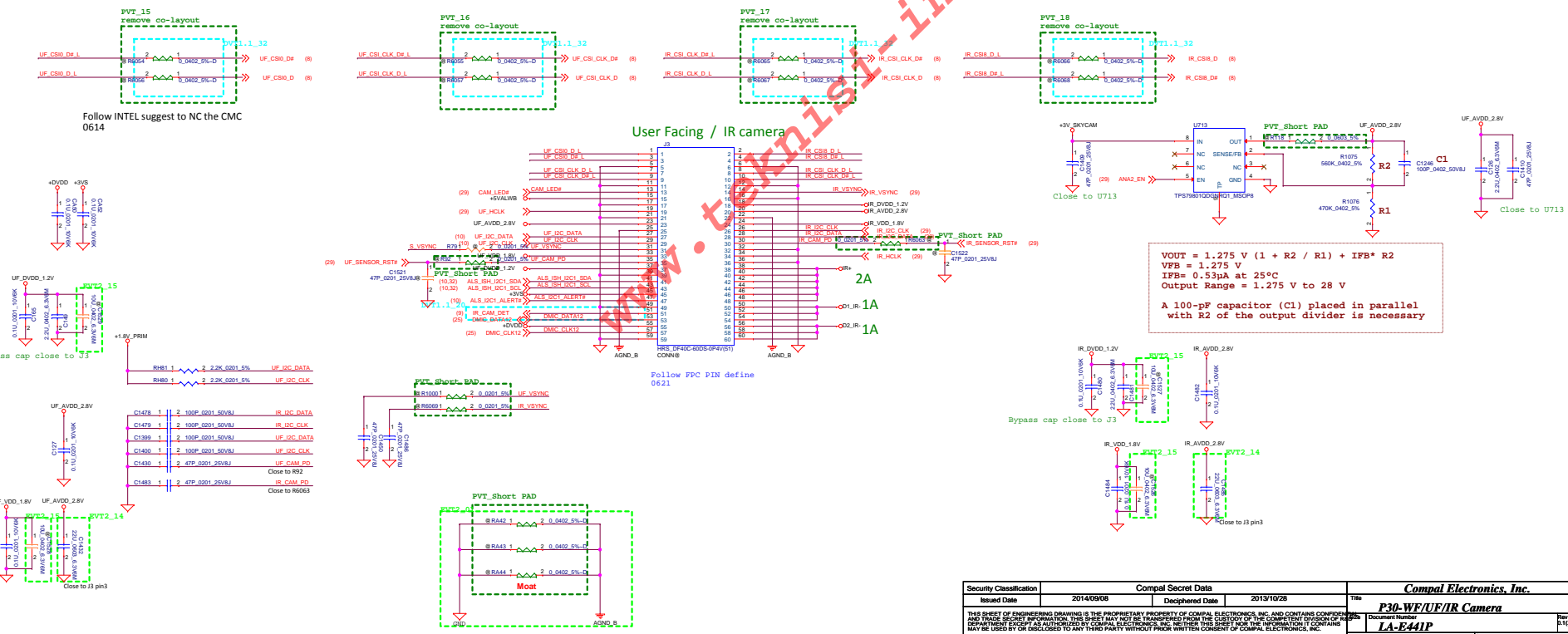
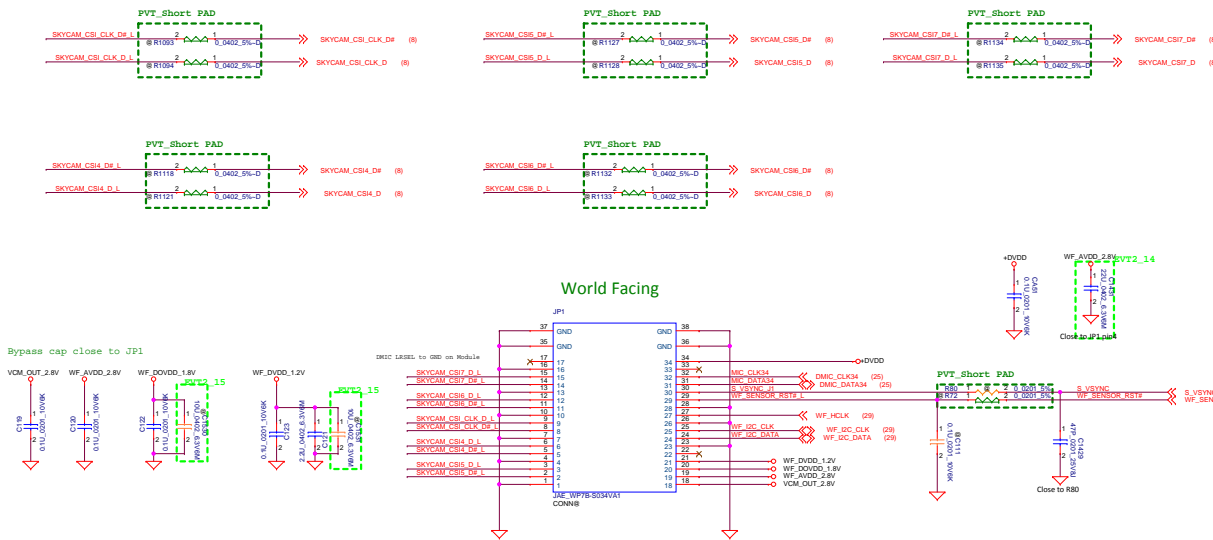
State#	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type	Port Configuration
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	HIGH	GND	GND	SSD - PCIe	N/A
2	GND	GND	HIGH	GND	WWAN - PCIe	0
3	GND	HIGH	HIGH	GND	WWAN - PCIe	1
4	GND	GND	GND	HIGH	WWAN - USB 3.0	0
5	GND	HIGH	GND	HIGH	WWAN - USB 3.0	1
6	GND	GND	HIGH	HIGH	WWAN - USB 3.0	2
7	GND	HIGH	HIGH	HIGH	WWAN - USB 3.0	3
8	HIGH	GND	GND	GND	WWAN - SSIC	0
9	HIGH	HIGH	GND	GND	WWAN - SSIC	1
10	HIGH	HIGH	HIGH	GND	WWAN - SSIC	2
11	HIGH	HIGH	HIGH	GND	WWAN - SSIC	3
12	HIGH	GND	GND	HIGH	WWAN - PCIe	2
13	HIGH	HIGH	GND	HIGH	WWAN - PCIe	3
14	HIGH	GND	HIGH	HIGH	DDP HCA - PCIe	N/A
15	HIGH	HIGH	HIGH	HIGH	No Module	N/A

Change to Key M CONN
0627



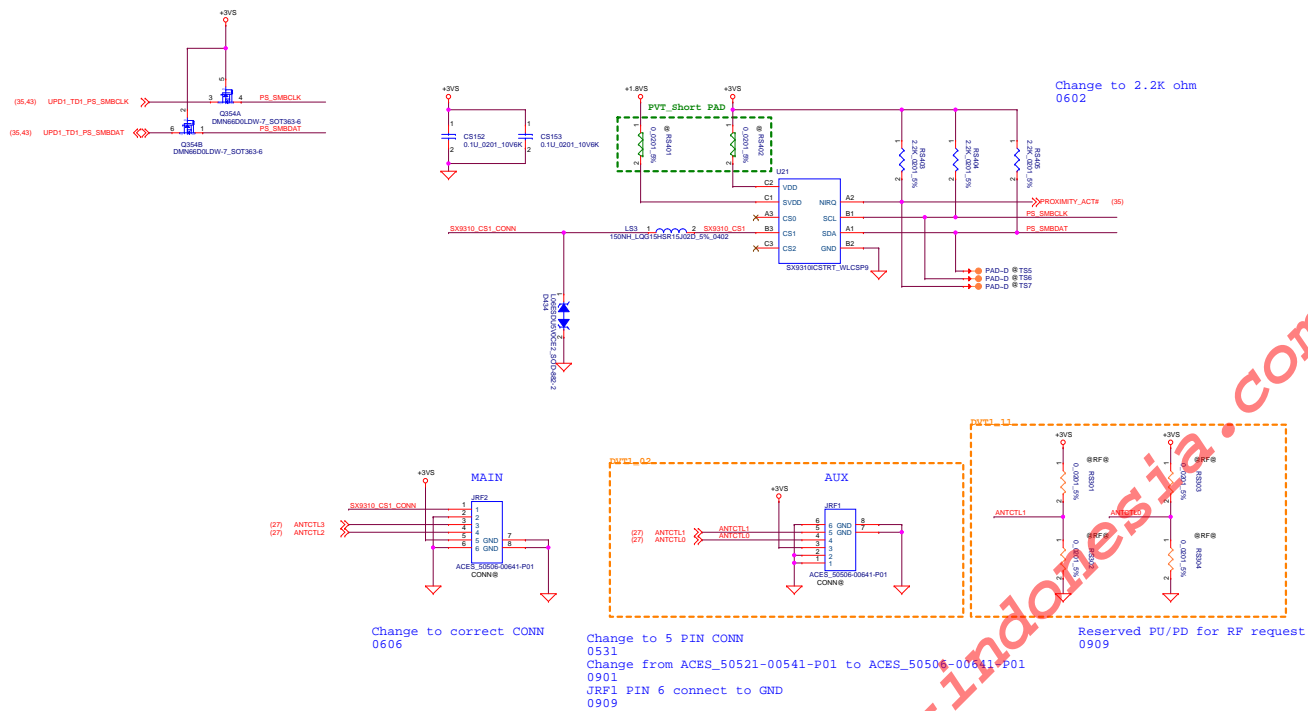


Follow INTEL suggest to remove the CMC
0614



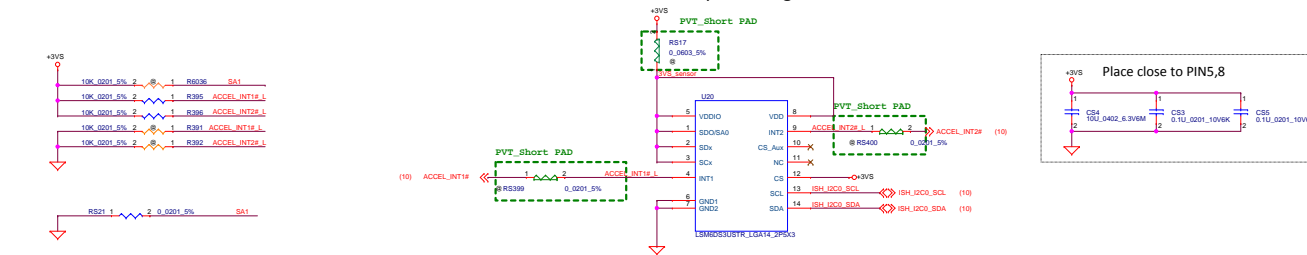
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SAR Proximity Sensor

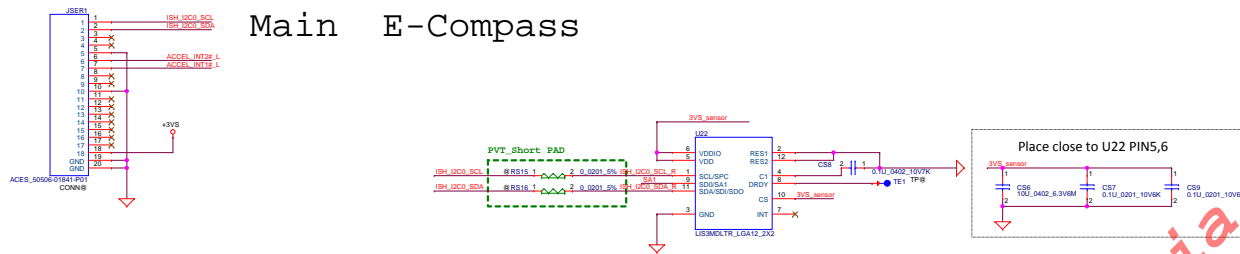


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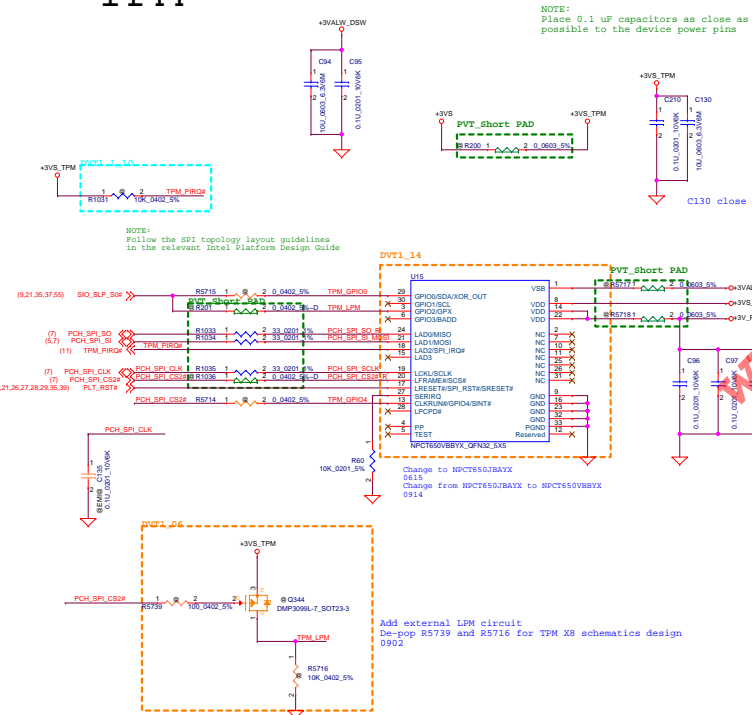
Accelerometer+Gyro & Magnetometer



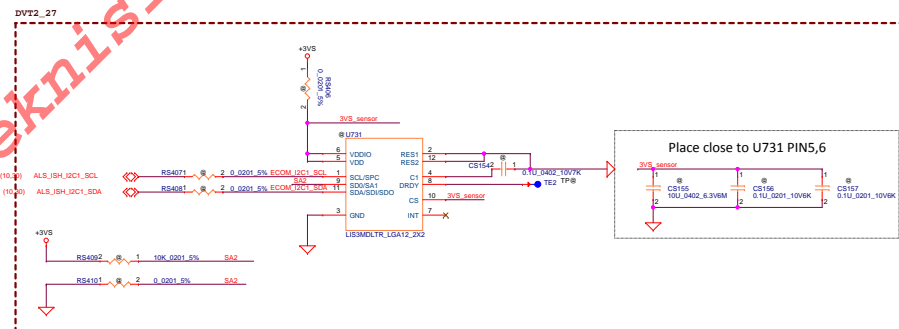
Main E-Compass



TPM



2nd E-Compass



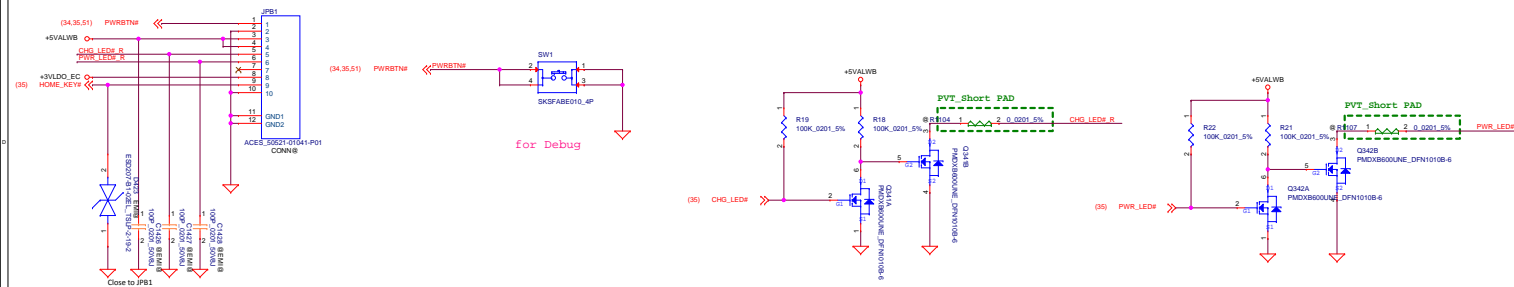
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Issued Date	2014/09/08	Deciphered Date	2013/10/28	Title	P32-e-Compass / TPM
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				Rev	0.10
				Drawn	Wednesday, March 26, 2017
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Docking CONN

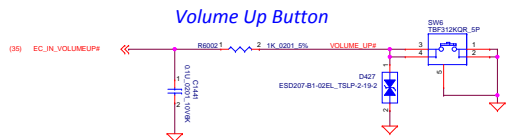


POGO_DET#	mode
0	NB Mode
1	Tablet Mod

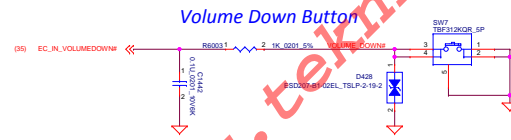
Power Button+ Home Key



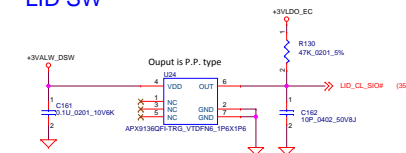
Volume Button

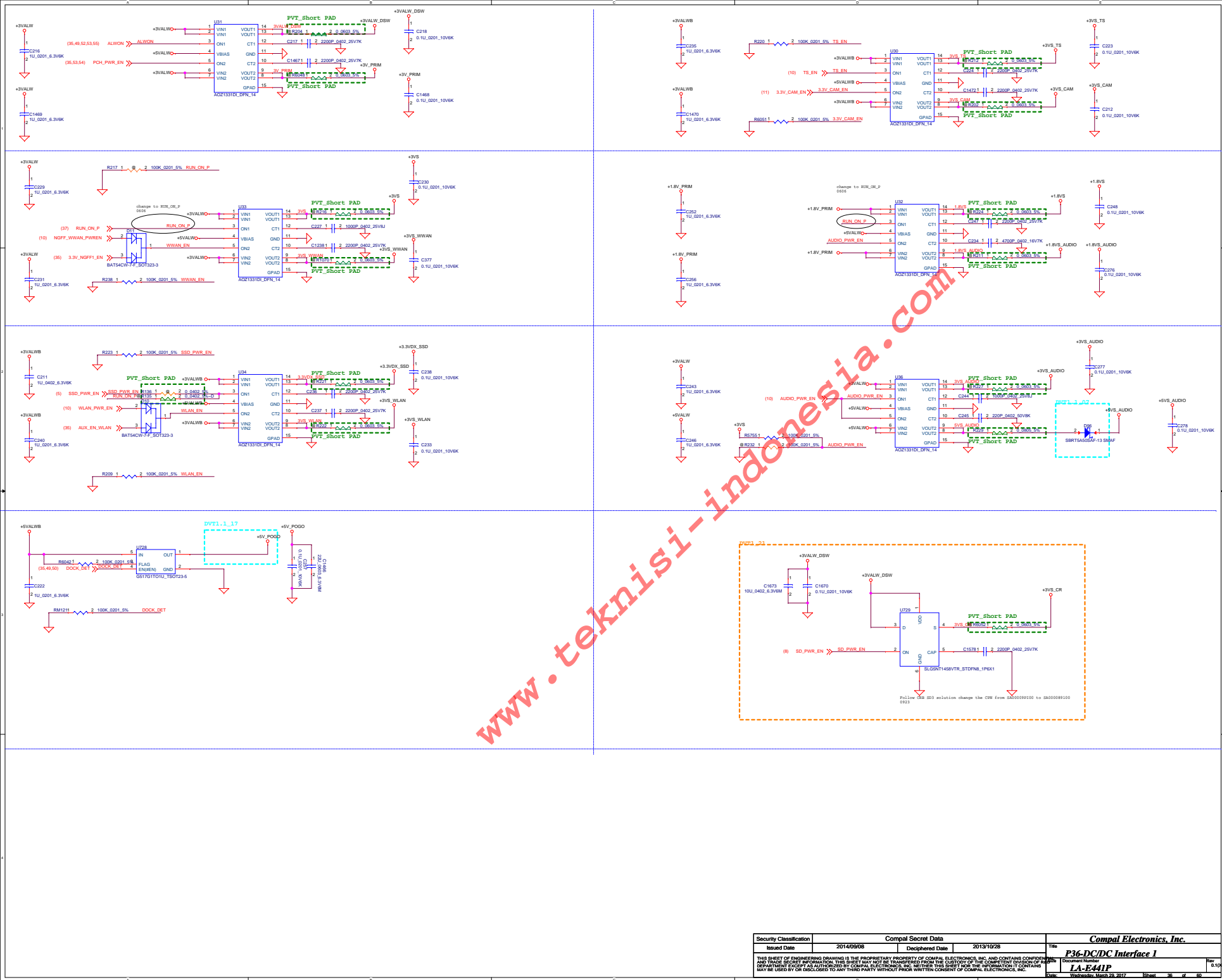


PU 10K resistor locate on EC side

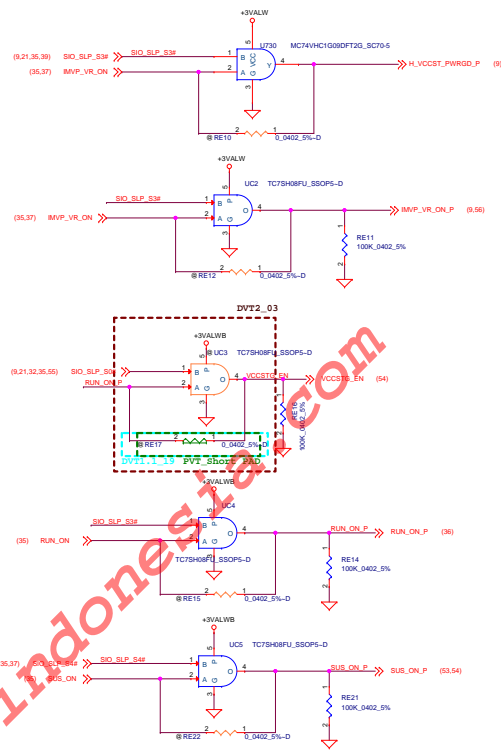
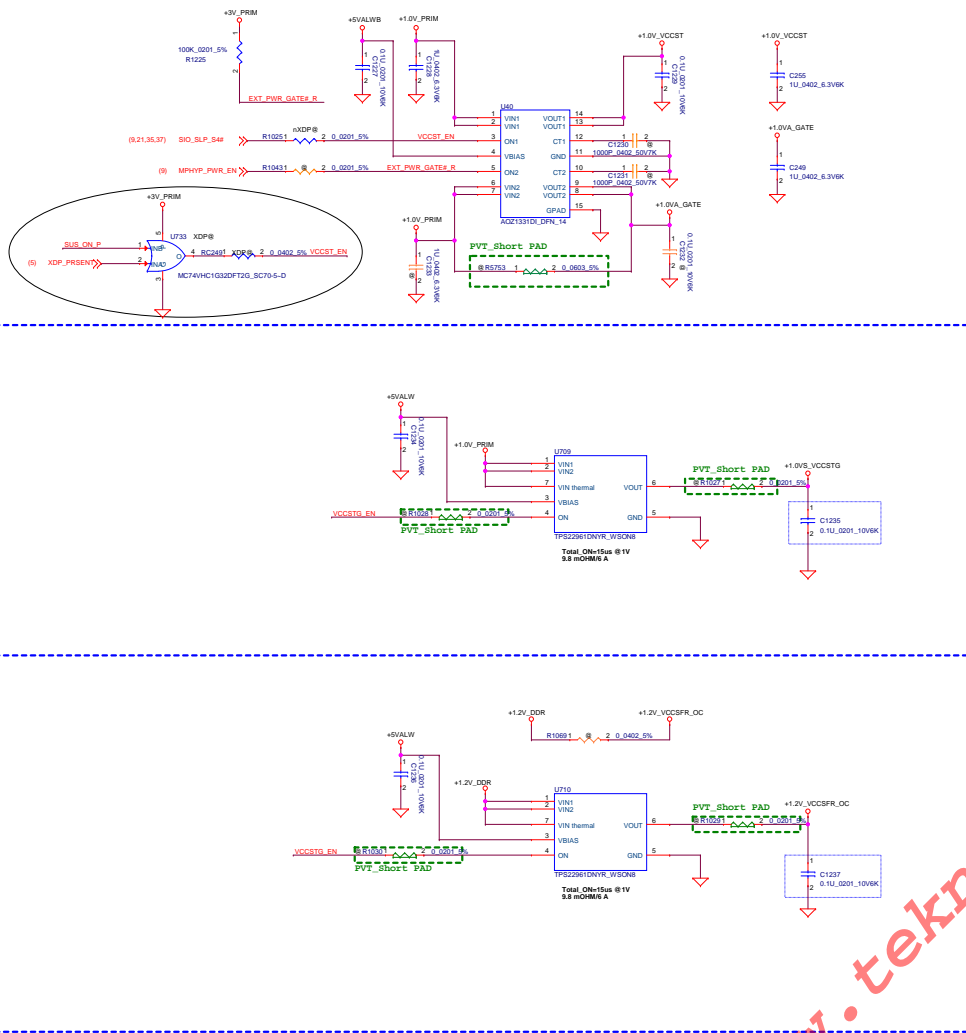


LID SW



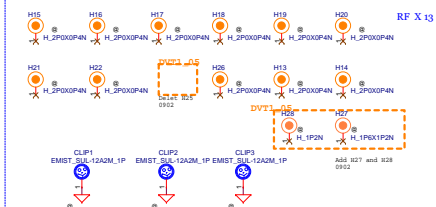
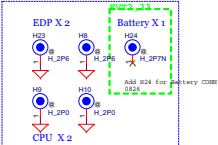
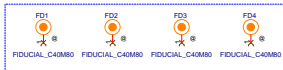


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				Document Number	Rev
				LA-E441P	0.10
				Date	Sheet
				Wednesday, March 26, 2017	36 of 60



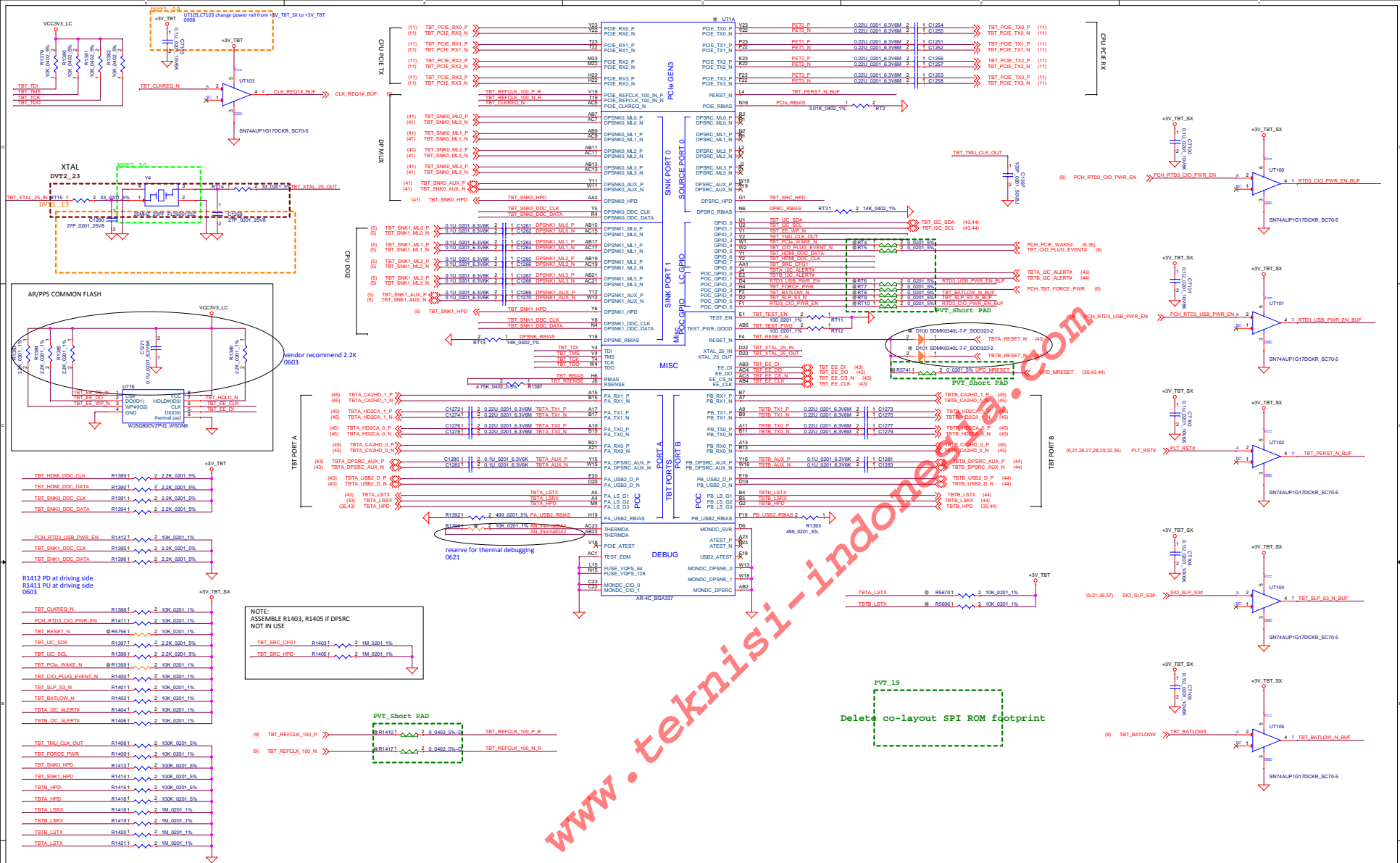
www.teknisi-indonesi.com

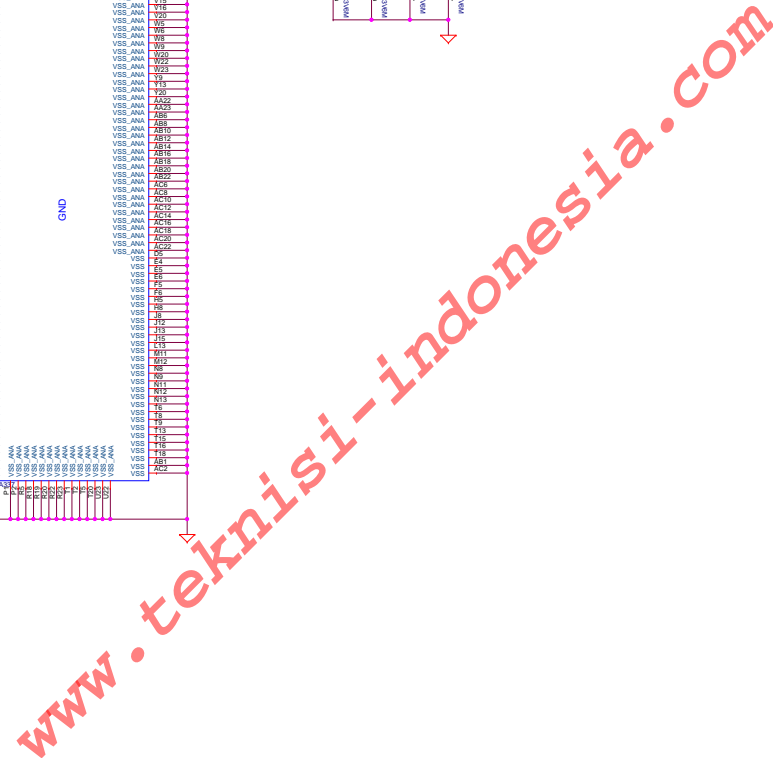
Screw Hole



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Security Classification	Compal Secret Data		Compal Electronics, Inc. P38-SCREWH / 10 Expander	
Issued Date	2014/09/08	Deciphered Date	2013/10/28	Title P38-SCREWH / 10 Expander LA-EM13
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Security Classification	Compal Secret Data		Compal Electronics, Inc. P40-AR TBT (2/2) PWR / VSS	
Issued Date	2014-09/08	Deciphered Date	2012/07/25	Title
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For Automatic Switching Mode (CFD0 = H):
SW = H: Port2 has higher priority when both ports are plugged (default)

Chip operational mode configuration:
Internal pull down at -150K Ω , 3.3V I/O.
L: Control switching mode (default)
H: Automatic switching mode

AUX interception disable for Port y (y=1,2)
Internal pull down at -150K Ω , 3.3V I/O.
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

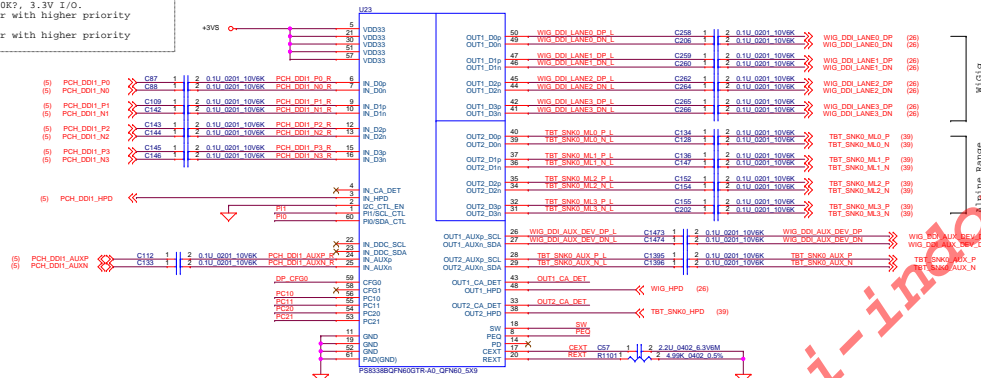
DP_MUX_SEL pin
Port switching control or priority configuration:
Internal pull down at -150K Ω , 3.3V I/O.
L: Port1 is selected or with higher priority (default)
H: Port2 is selected or with higher priority

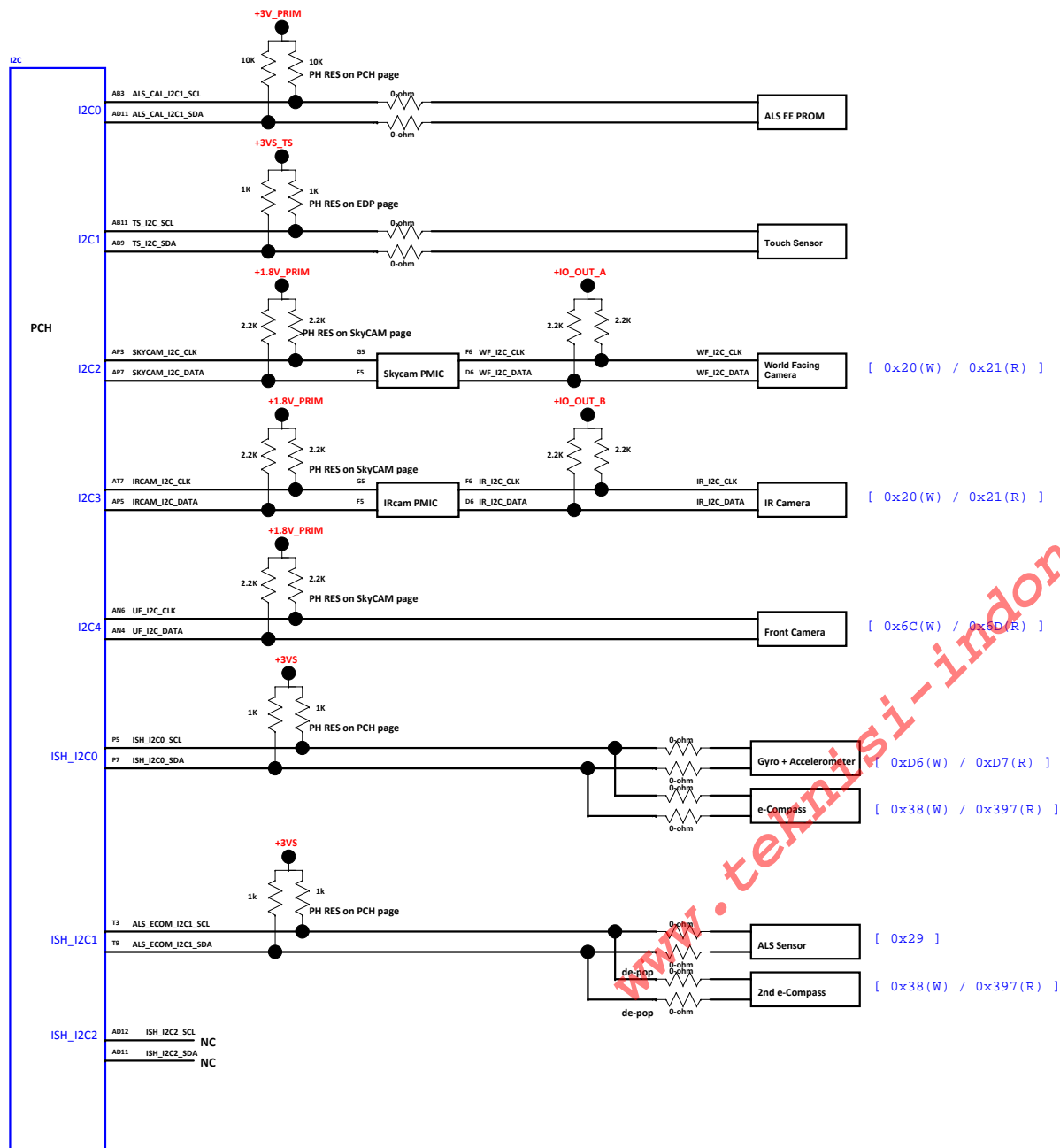
Automatic EQ disable:
Internal pull down at -150K Ω , 3.3V I/O
L: Automatic EQ enable (default)
H: Automatic EQ disable

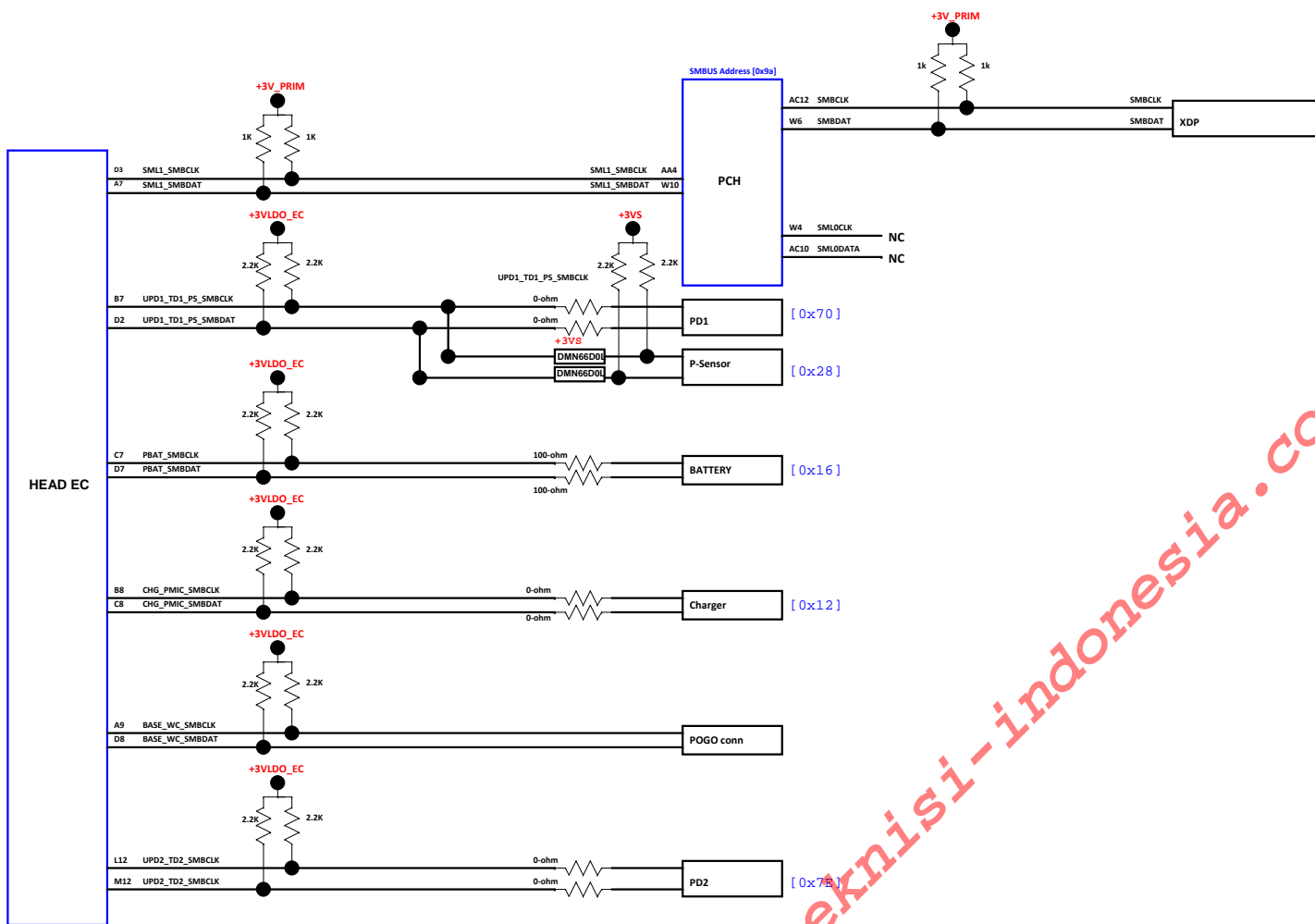
Output swing adjustment for Port y (y=1,2).
Internal pull down at -150K Ω , 3.3V I/O.
L: default
H: +20%
M: -16.7%

Auto test enable:
Internal pull down at -150K Ω , 3.3V I/O.
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

Programmable input equalization levels: Internal pull down at -150K Ω , 3.3V I/O.
L: default, LEO, compensate channel loss up to 11.5dB @ HBR2
H: HEO, compensate channel loss up to 14.5dB @ HBR2
M: LEO, compensate channel loss up to 8.5dB @ HBR2

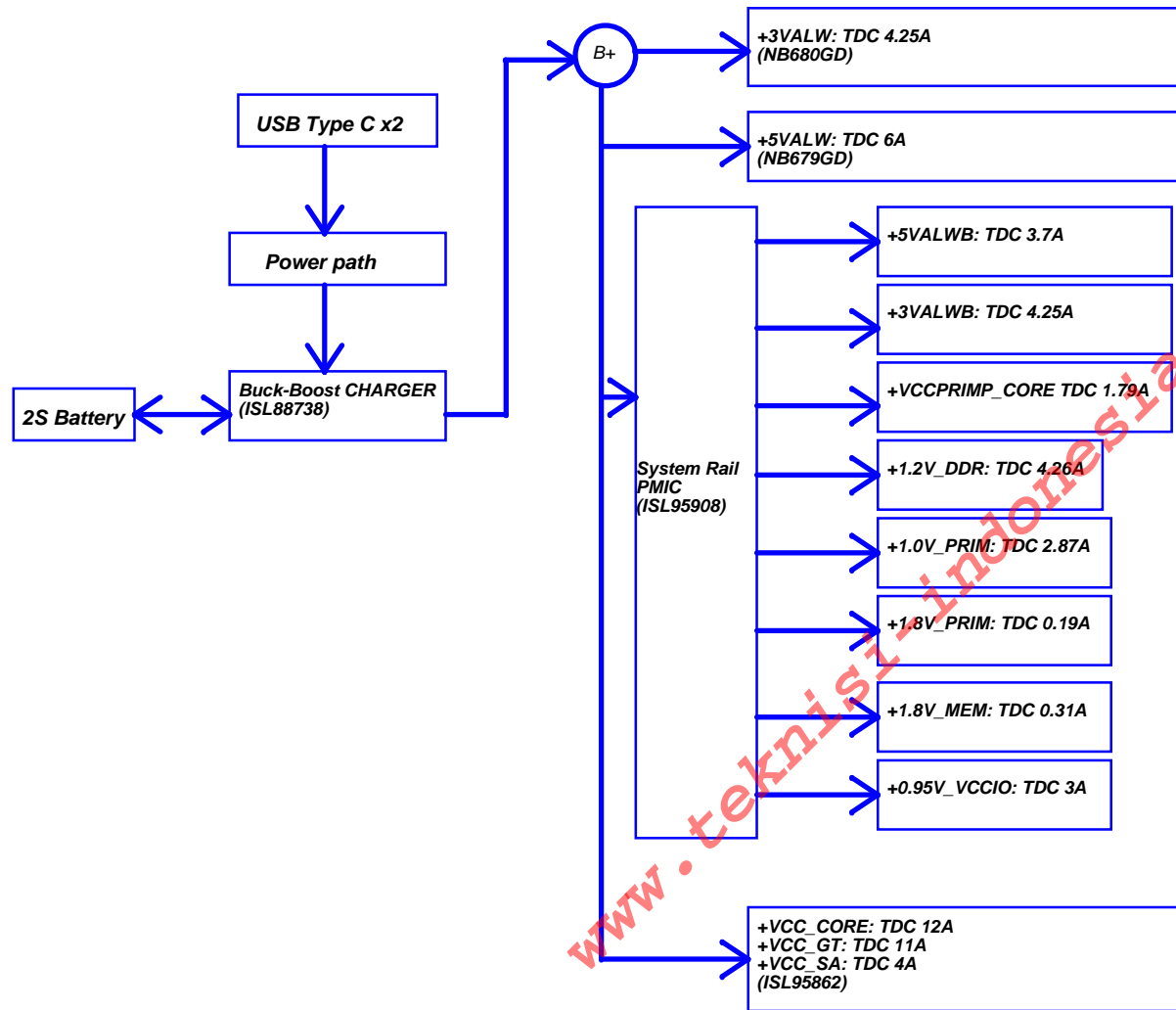




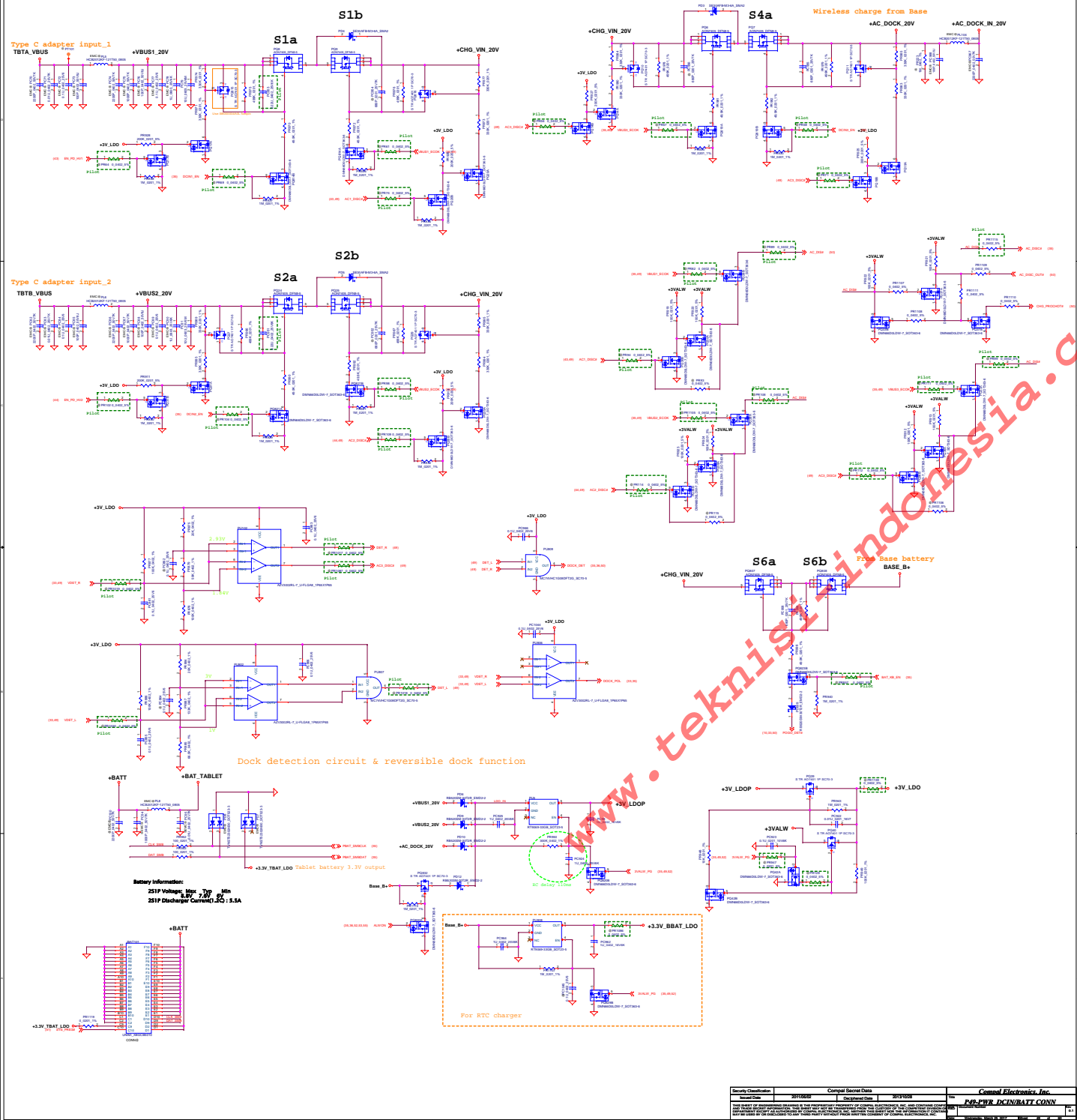


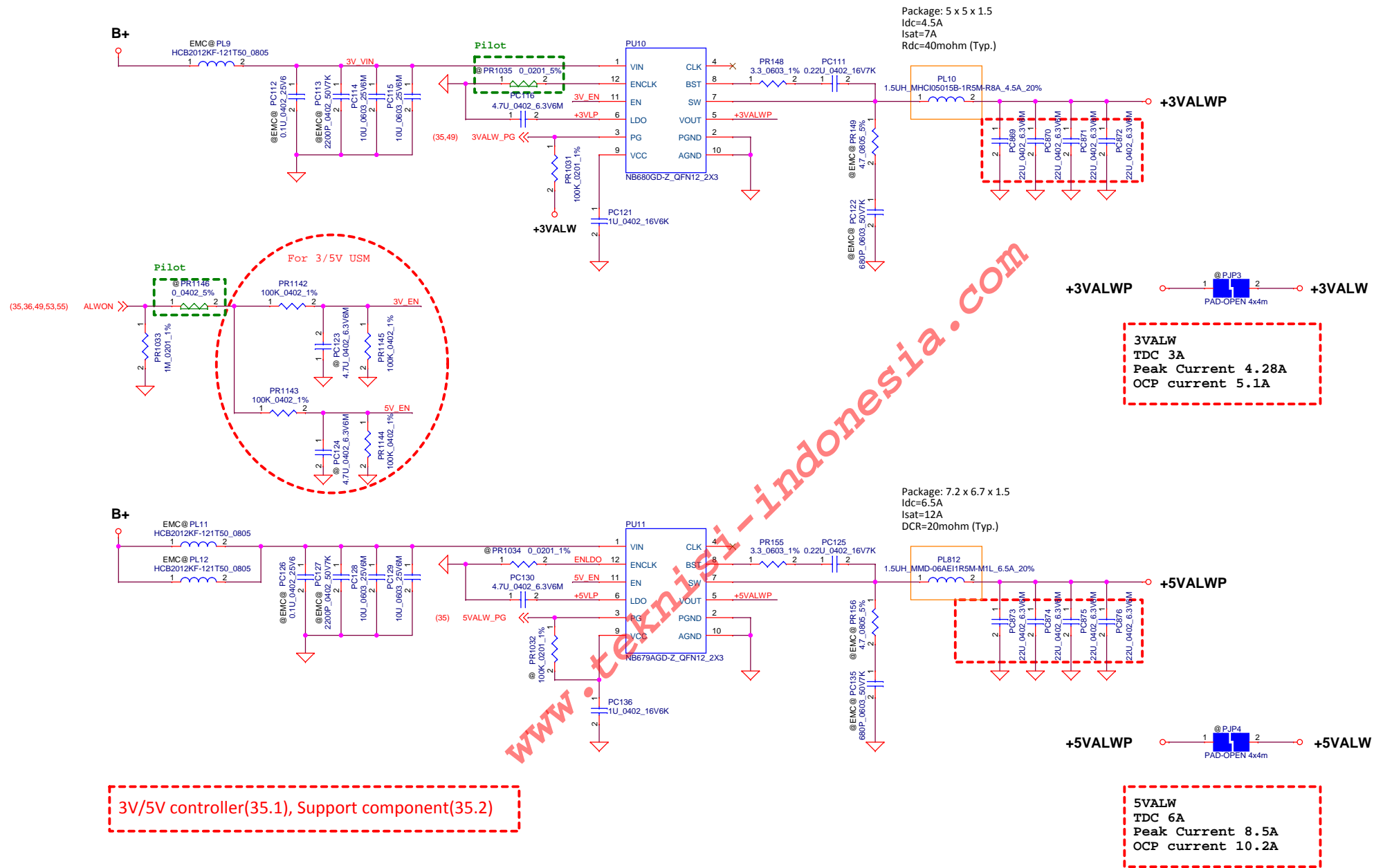
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ASPEN Power Block - Tablet

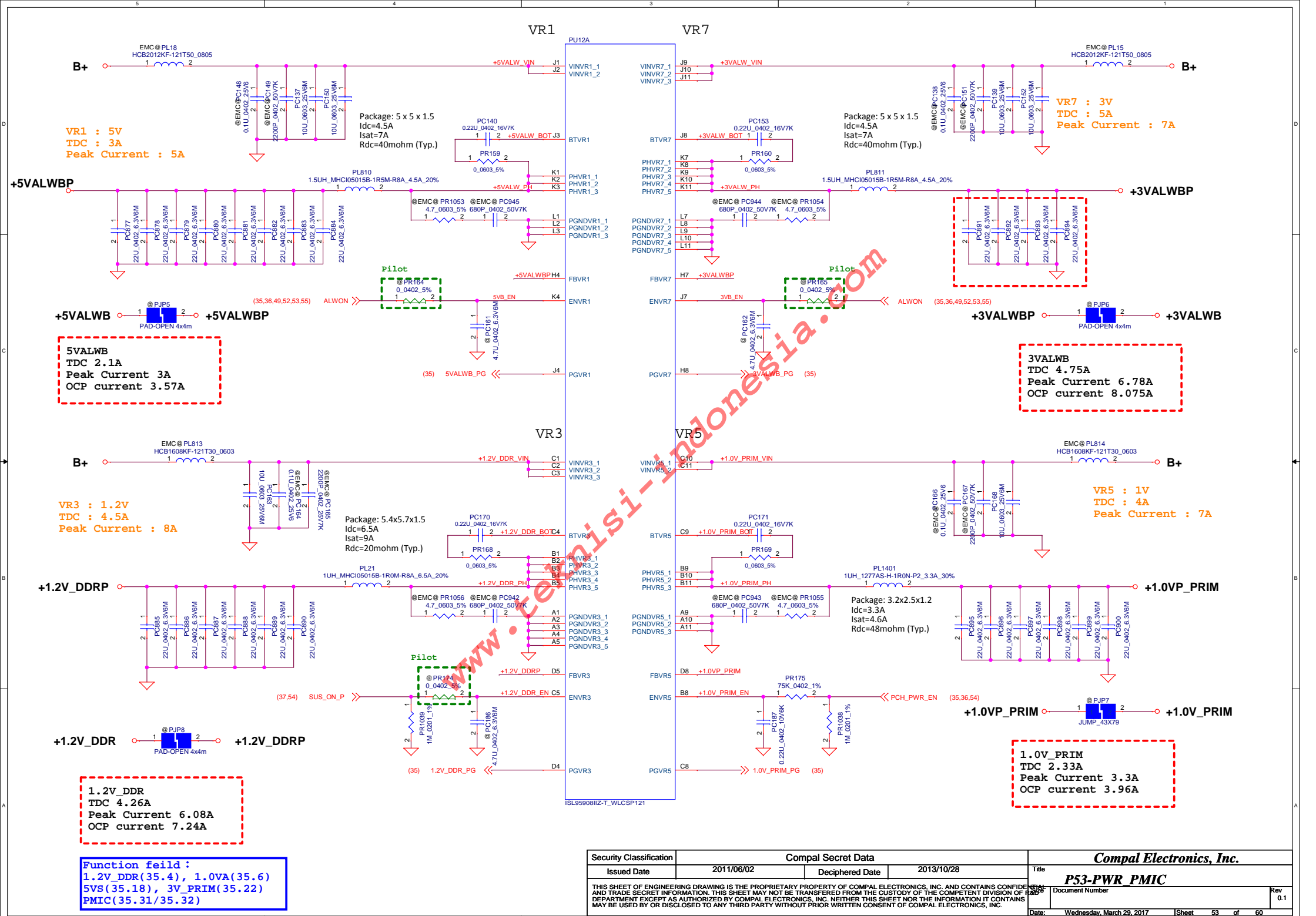


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/08/20	Deciphered Date	2015/08/20	Title	P48-PWR POWER BLOCK DIAGRAM
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P52-PWR +3V(NB680)/+5V(NB679)
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VR6 : 1.8V
TDC : 2A
Peak Current : 2.5A

VR8 : 1.0V
TDC : 1A
Peak Current : 1.5A

1.8V_PRIM
TDC 0.16A
Peak Current 0.23A
OCP current 0.28A

VCCPRIM_CORE
TDC 0.77A
Peak Current 1.1A
OCP current 1.31A

VR4 : 1.8V
TDC : 1A
Peak Current : 1A

VR2 : 0.95V
TDC : 2.5A
Peak Current : 3A

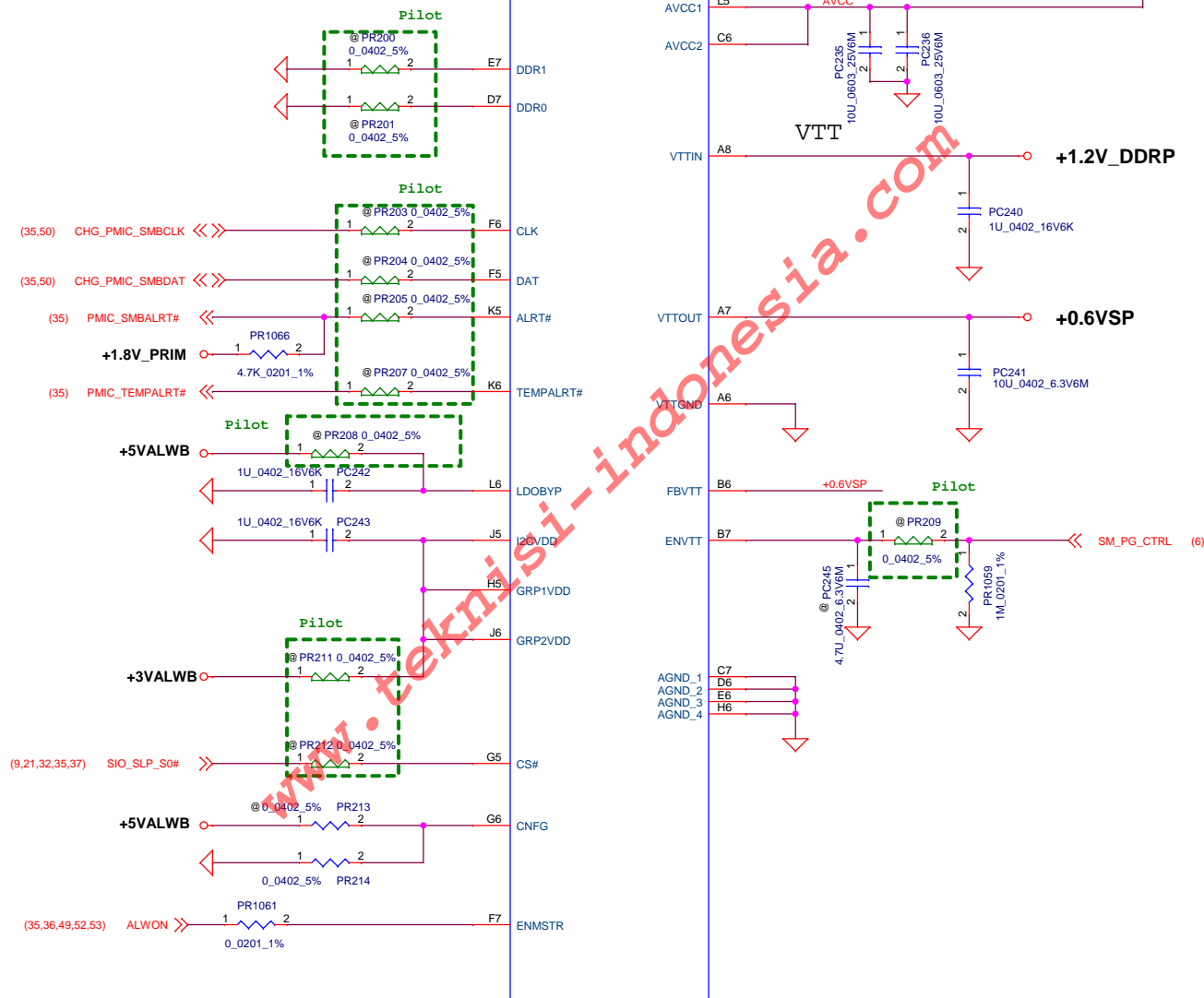
1.8V_MEM
TDC 0.1A
Peak Current 0.14A
OCP current 0.17A

0.95VS_VCCIO
TDC 2.1A
Peak Current 3A
OCP current 3.57A

Function feild:
1.0V_PRIM(35.8), 0.95VS_VCCIO(35.12)
1.8VA(35.14), 1.8VU(35.16)
PMIC(35.31/35.32)

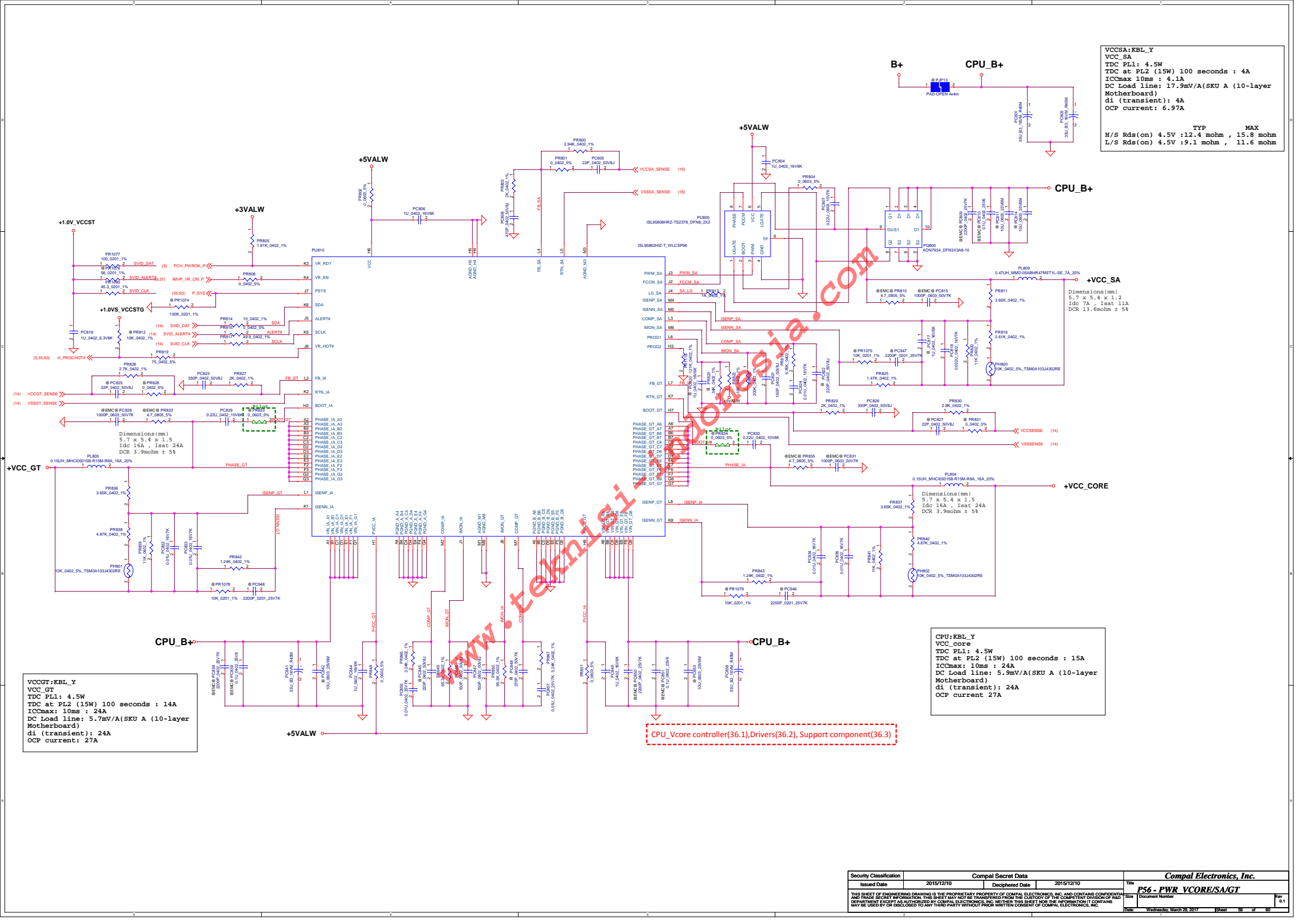
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P54-PWR_PMIC
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DDR[1:0]	VR3	VTT
[0:0]	1.2	0.6
[0:1]	1.25	0.625
[1:0]	1.35	0.675
[1:1]	1.5	0.75



Function feild :
PMIC (35.31/35.32)

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VCCSA:KBL_Y
VCC_SA
TDC PL1: 4.5W
TDC at PL2 (15W) 100 seconds : 4A
IC_{max} 10ms : 4.1A
DC Load line: 17.9mV/A (SKU A (10-layer Motherboard))
di (transient): 4A
OCF current: 6.97A

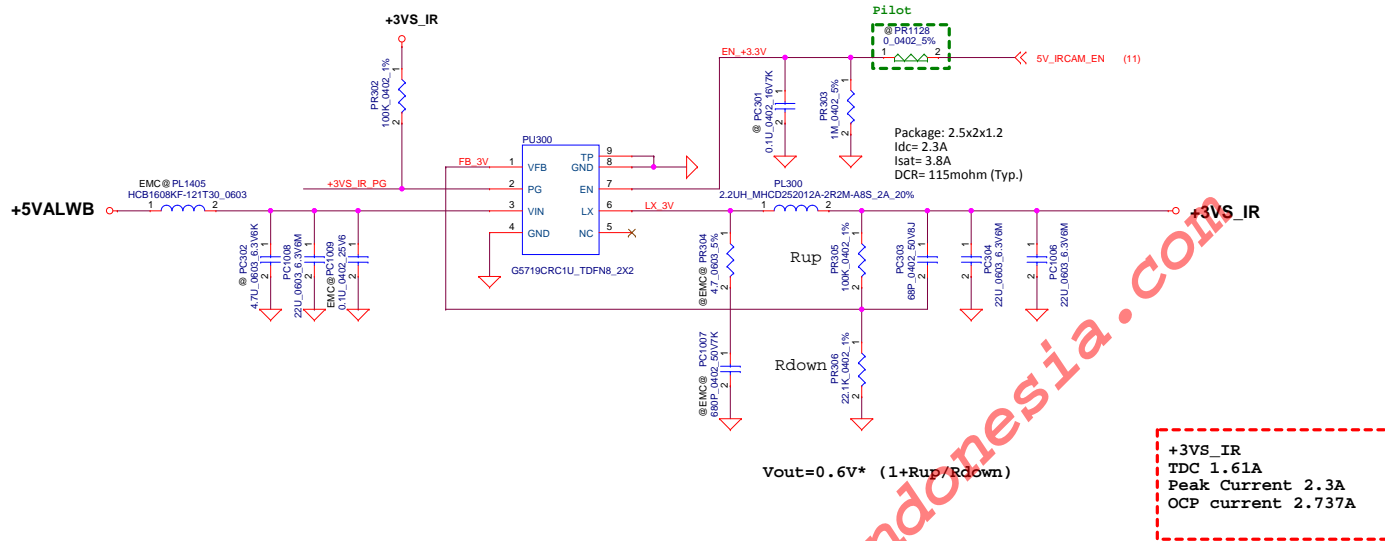
TYP MAX
H/S R_{ds}(on) 4.5V :12.4 mohm , 15.8 mohm
L/S R_{ds}(on) 4.5V :9.1 mohm , 11.6 mohm

Dimensions (mm)
5.7 x 5.4 x 1.2
I_{dc} 7A , I_{sat} 11A
DCR 13.6mohm ± 5%

CPU:KBL_Y
VCC_core
TDC PL1: 4.5W
TDC at PL2 (15W) 100 seconds : 15A
IC_{max} : 10ms : 24A
DC Load line: 5.9mV/A (SKU A (10-layer Motherboard))
di (transient): 24A
OCF current 27A

VCCGT:KBL_Y
VCC_GT
TDC PL1: 4.5W
TDC at PL2 (15W) 100 seconds : 14A
IC_{max} : 10ms : 24A
DC Load line: 5.7mV/A (SKU A (10-layer Motherboard))
di (transient): 24A
OCF current: 27A

CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3)

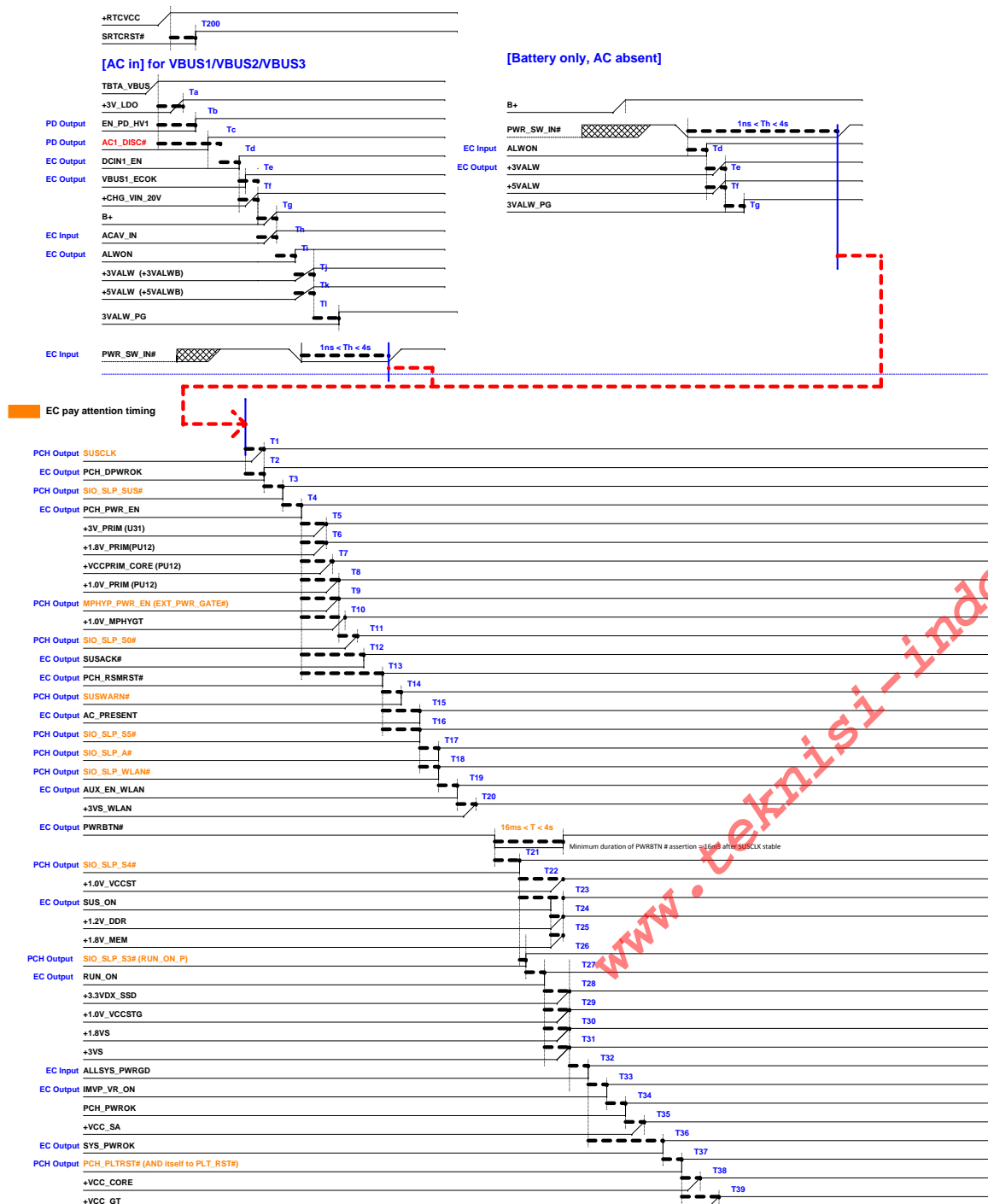


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				Document Number	Rev 0.1
				Date: Wednesday, March 29, 2017	Sheet 58 of 60

Discrete Power On Sequence

[AC in]

[Battery only, AC absent]



ITEM	Measure Point	Time
Ta	+VBUS_PD_20V	To
Tb	+3V_LDO	To
Tc	EN_PD_HV1	To
Td	AC1_DISC#	To
Te	DCIN1_EN	To
Tf	VBUS1_ECOK	To
Tg	+CHG_VIN_20V	To
Th	B+	To
Ti	ACAV_IN	To
Tj	ALWON	To
Tk	+3VALW	To
Tl	+5VALW	To

ITEM	Measure Point	Time
Tc	B+	To
Th	POWER_SW_IN#	To
Td	POWER_SW_IN#	To
Te	ALWON	To
Tf	ALWON	To
Tg	+3VALW	To

ITEM	Measure Point	Time
T1	DSW_ON	To
T2	+3VALW_DSW	To
T3	+3VALW_DSW	To
T4	PCH_DPWRWK	To
T5	SIO_SLP_SUS#	To
T6	PCH_PWR_EN	To
T7	PCH_PWR_EN	To
T8	PCH_PWR_EN	To
T9	PCH_PWR_EN	To
T10	PCH_PWR_EN	To
T11	PCH_PWR_EN	To
T12	EXT_PWR_GATE#	To
T13	PCH_PWR_EN	To
T14	PCH_PWR_EN	To
T15	PCH_RSMRST#	To
T16	PCH_RSMRST#	To
T17	PCH_RSMRST#	To
T18	SIO_SLP_S5#	To
T19	SIO_SLP_S5#	To
T20	SIO_SLP_WLAN#	To
T21	AUX_EN_WLAN	To
T22	SIO_PWRBTN#	To
T23	SIO_SLP_S4#	To
T24	SUS_ON_EC	To
T25	SUS_ON_EC	To
T26	SUS_ON_EC	To
T27	SIO_SLP_S4#	To
T28	SIO_SLP_S3#	To
T29	RUN_ON_EC	To
T30	RUN_ON_EC	To
T31	RUN_ON_EC	To
T32	RUN_ON_EC	To
T33	RUN_ON_EC	To
T34	RUN_ON_EC	To
T35	+3VS	To
T36	RUNPWROK	To
T37	VR_ON	To
T38	VCCORE_PG	To
T39	VR_ON	To
T40	SYS_PWROK	To
T41	PCH_PLTRST#	To
T42	PCH_PLTRST#	To

update

